

Compal confidential

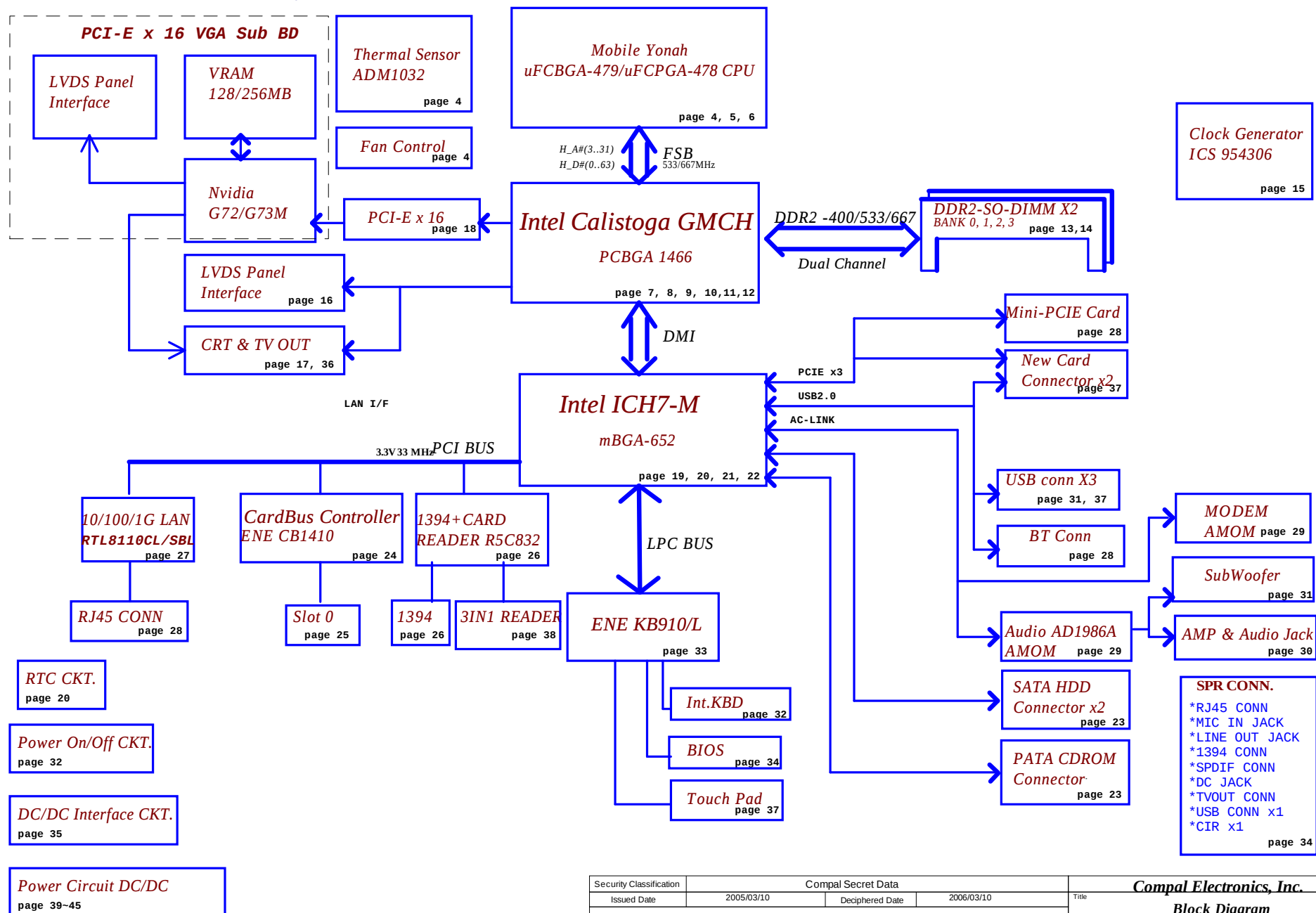
HGT30/31 Schematics Document

Mobile Yonah uFCPGA with Intel Calistoga_GM/PM+ICH7-M core logic

2006-02-15

REV:0.3

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
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[illegible]

+3VALW	KB910L SB RTL8110SBL/CL	mA 160mA
+CPU_CORE	CPU	36A
+VCCP	CPU NB	2.5A 9.8A (14.7A)
+5VS	EXPRESS CARD HDD ODD MDC APA2066 TPA0211 AD1986 USB PORT * 6	1A 1.5A 1.8A 300mA 1A mA 70mA 3A
+3VS	NB EXPRESS CARD CLK_GEN LCDVCC VGA CARD (G7XM) SB R5C832 BIOS ROM KB910L CB1410	480mA 1A 200mA 1A 655mA 680mA mA 15mA 200mA mA
+2.5VS	VGA CARD (G7XM) NB	130mA (143mA)
+1.8V	DDR2_DIMM NB (667Mhz)	8A 3.1A
+1.8VS	GDDR2 VGA CARD (G7XM)	6A 4.06A
+0.9VREF	DDR2_DIMM	10mA
+0.9VS	GDDR2 DDR2_DIMM	1A 2A
+1.5V	SB	40mA
+1.5VS	NB SB MiniCard EXPRESS CARD VGA CARD (G7XM)	8.9A(13.8A) 3.8A 1A 0.65A 2A

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ	
CARD BUS CB1410	AD20	2	PCI_PIRQA#	
CARD READER & 1394 R5C832	AD22	0	PCI_PIRQG#	PCI_PIRQH#
LAN CONTROLLER RTL8110SBL/CL	AD17	3	PCI_PIRQF#	

LANE	DEVICE
1	Express Card
2	Mini Card

PORT	DEVICE
0	LEFT SIDE
1	BLUE TOOTH
2	RIGHT SIDE
3	NC
4	RIGHT SIDE
5	NC
6	NC

DEVICE	ADDRESS R/W
AT24C16AN	A3/A2 H
SMART BATTERY	17/16 H
KB910/L (SM1-Pulled-Up 5V) KB910/L (SM2-Pulled-Up 3.3V) G7xPM (I2CC-Pulled-Up 3.3V)	
ADM1032AR	99/98 H
G781-1 (RESERVED)	9B/9A
ICH7M SM Bus ICS9LP3R325AKLFT	
D3/D2 H	(3.3V)
DDR II DIMM0	A1/A0 H (3.3V)
DDR II DIMM1	A3/A2 H (3.3V)
Express Card	NC (2.5V)
Mini-Express	NC (2.5V)

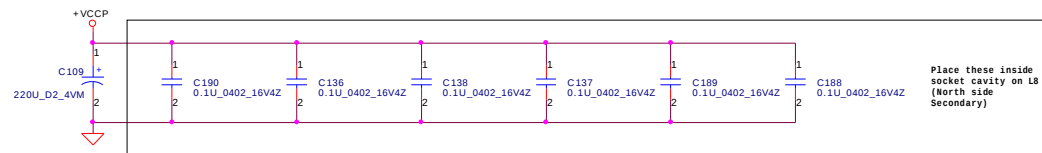
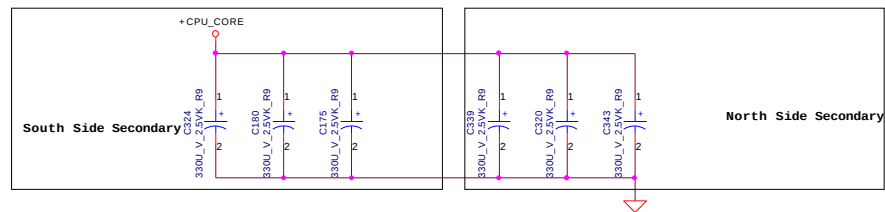
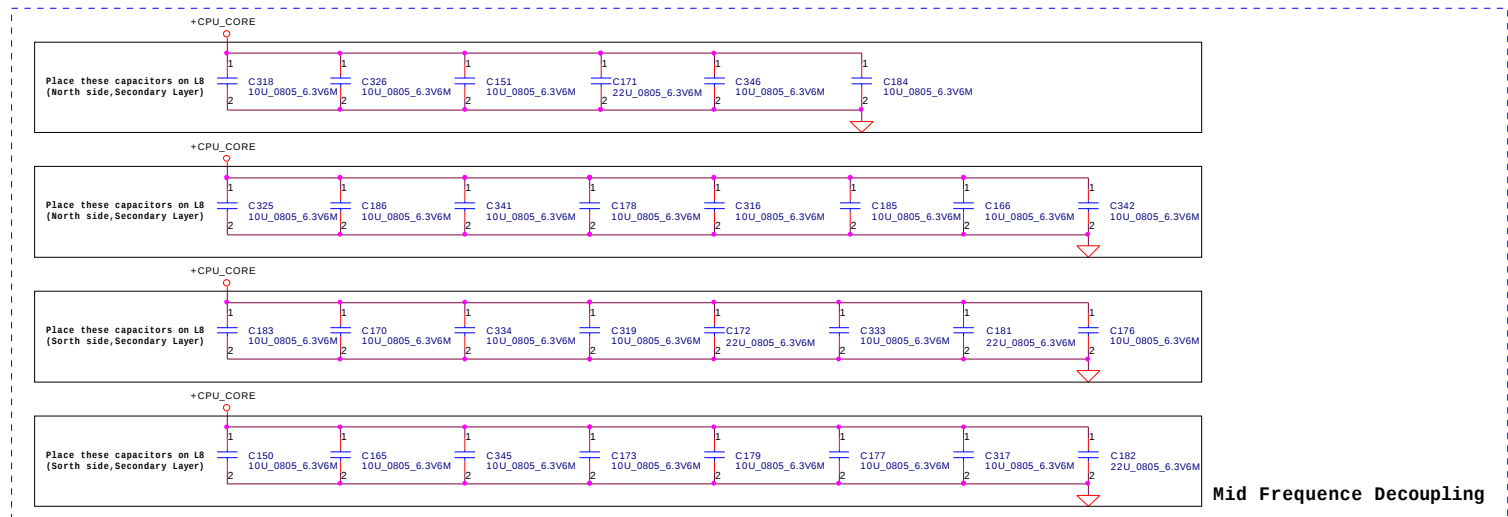
MARK	FUNCTION
@	NC FOR ALL
EXP@	PCI-E NEW CARD
BT@	BLUE TOOTH
UMA@	Internal 945GM
VGA@	External 67xm
SUBWOOFER@	SUBWOOFER
HGT30@	HGT30
CB@	PCMCTA/CARD BUS
GIGA@	8110SBL (SCL)Giga LAN
10/100@	8110CL 10/100Mb LAN

power plane State S4 : STD S5 : S0FT OFF	+B LD03 LD05	+5VALW +3VALW	+1.8V +5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +VGA CORE +1.2VS +0.9VS +CPU CORE +VCCP
S0	0	0	0	0
S1	0	0	0	0
S3 : STR	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

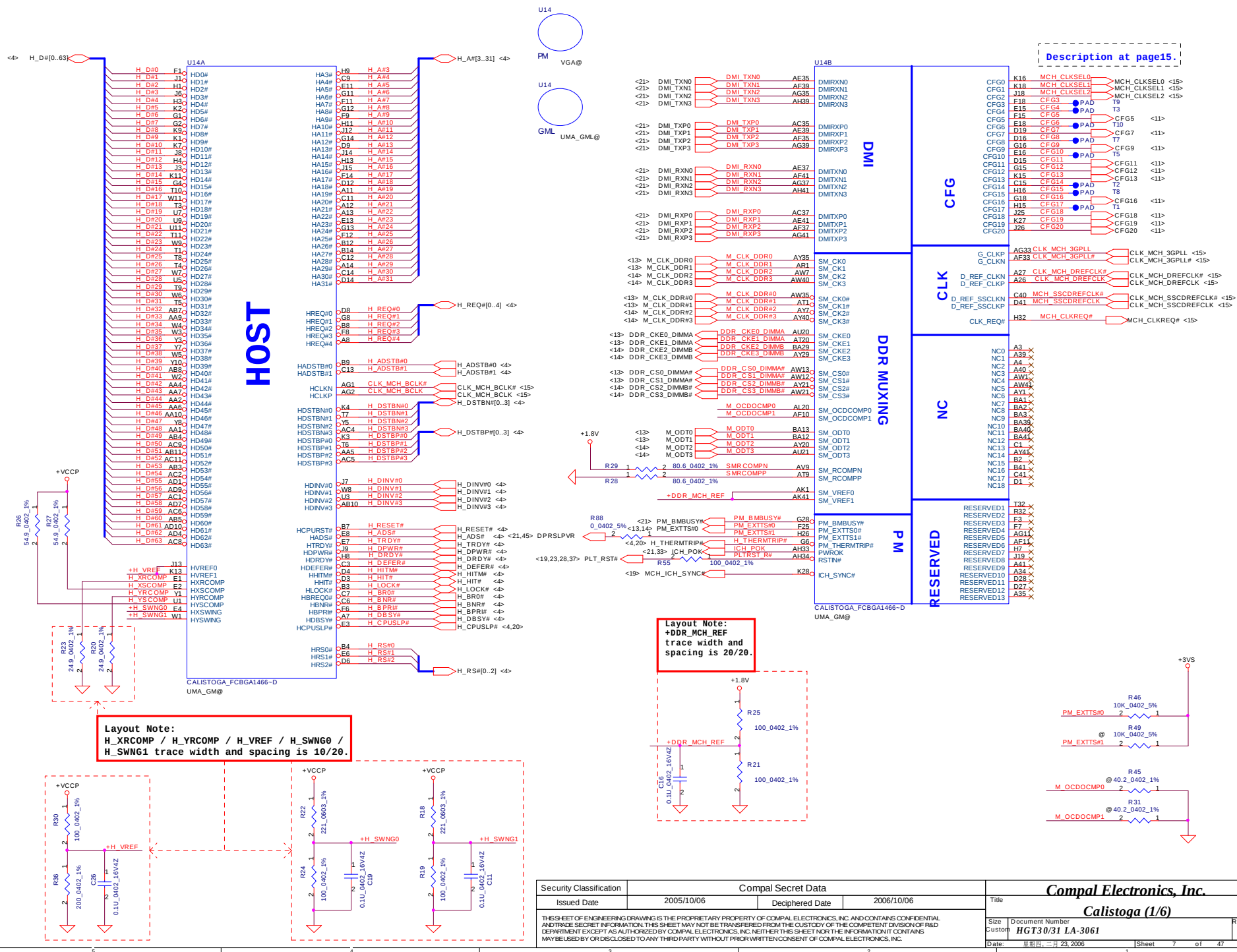
MB ID	P NAME
0	HGT-30
1	HGT-31

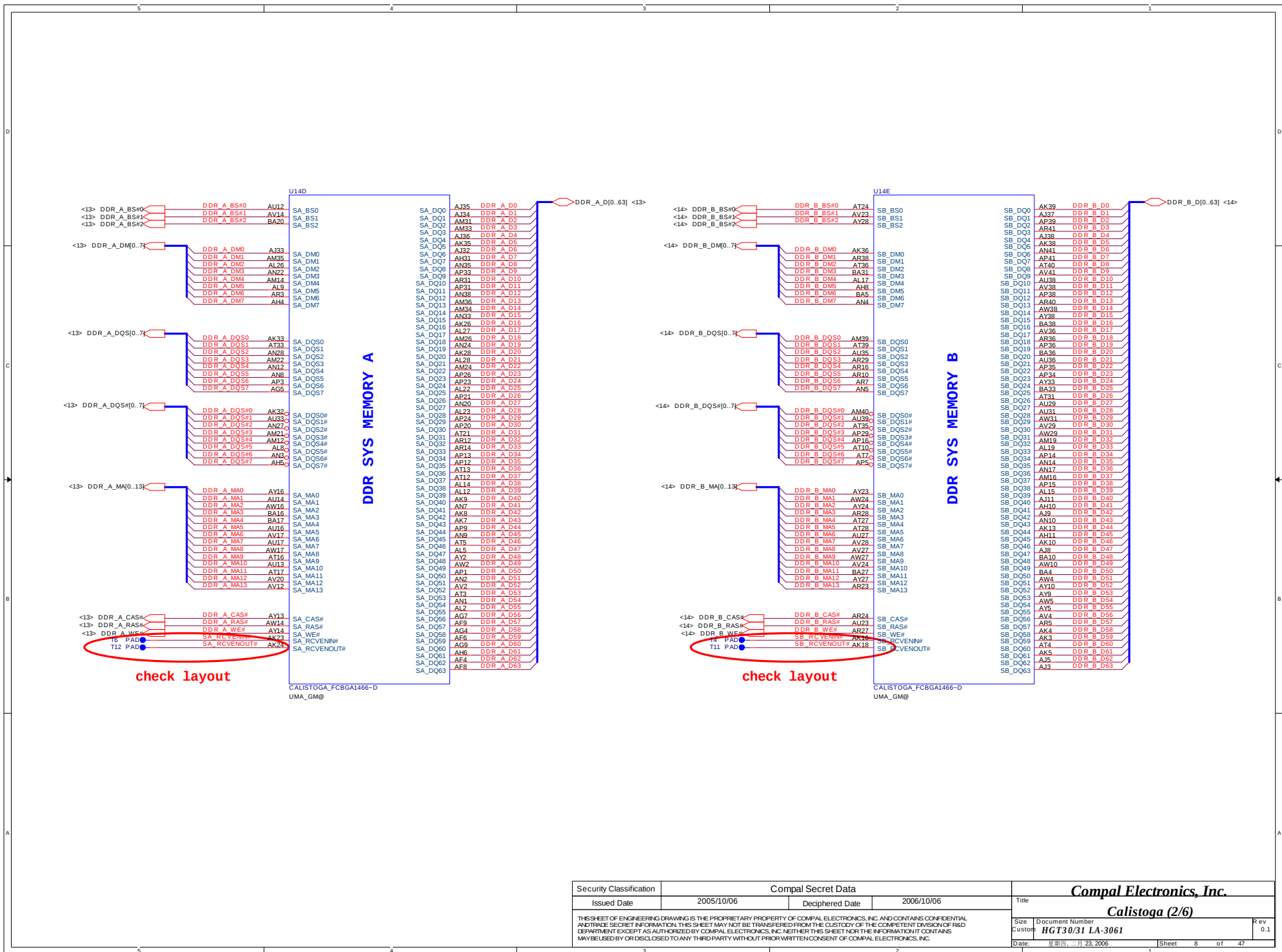
ID	MB REV#	R115(Rb)	Vab
0	R01 (EVT)	0	0'
1	R02 (DVT)	8.2K	0.25'
2	R03	18K	0.50'
3	R04	33K	0.82'
4		56K	1.19'
5		100K	1.65'
6		200K	2.20'
7		NC	3.30'

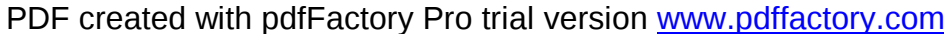
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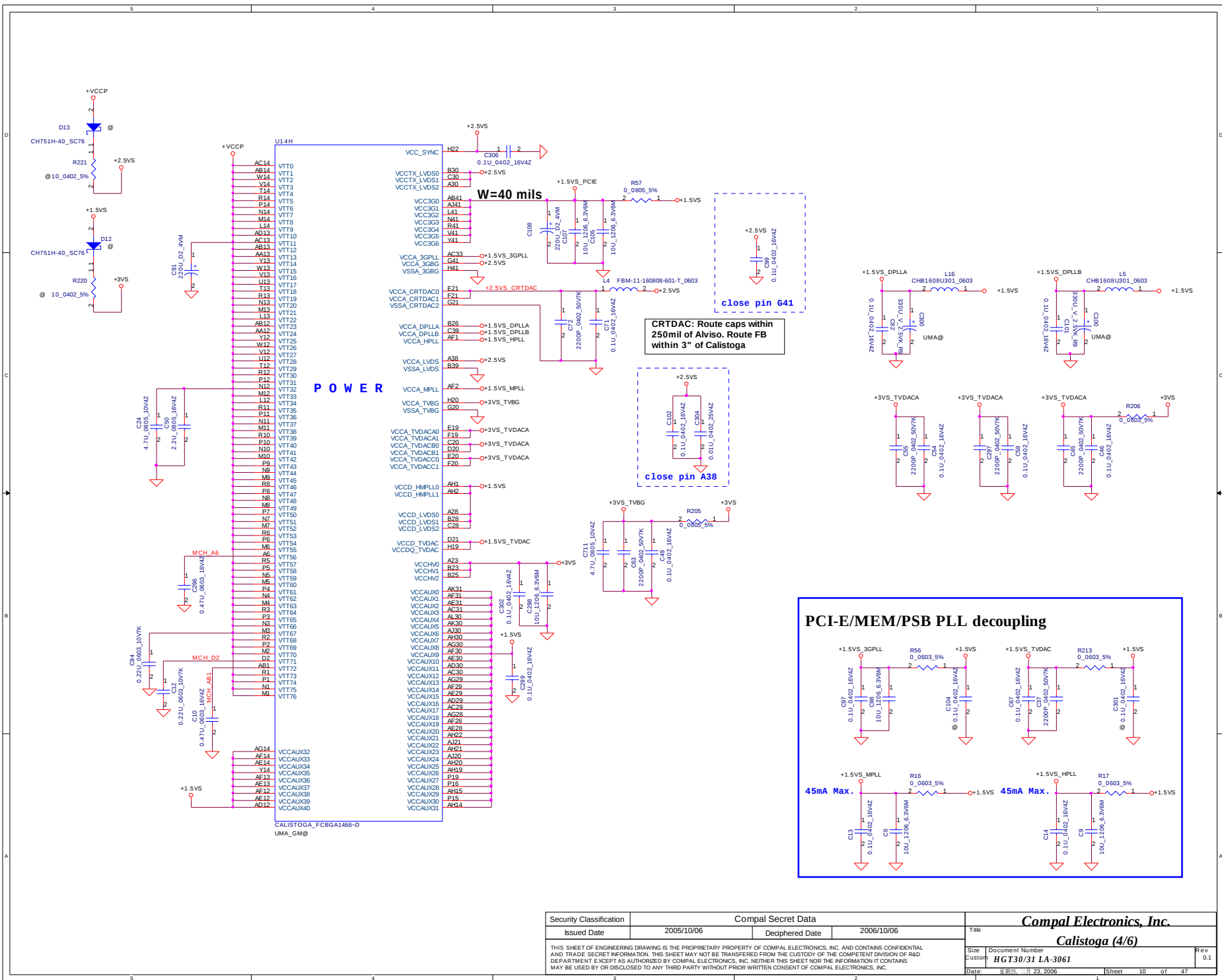


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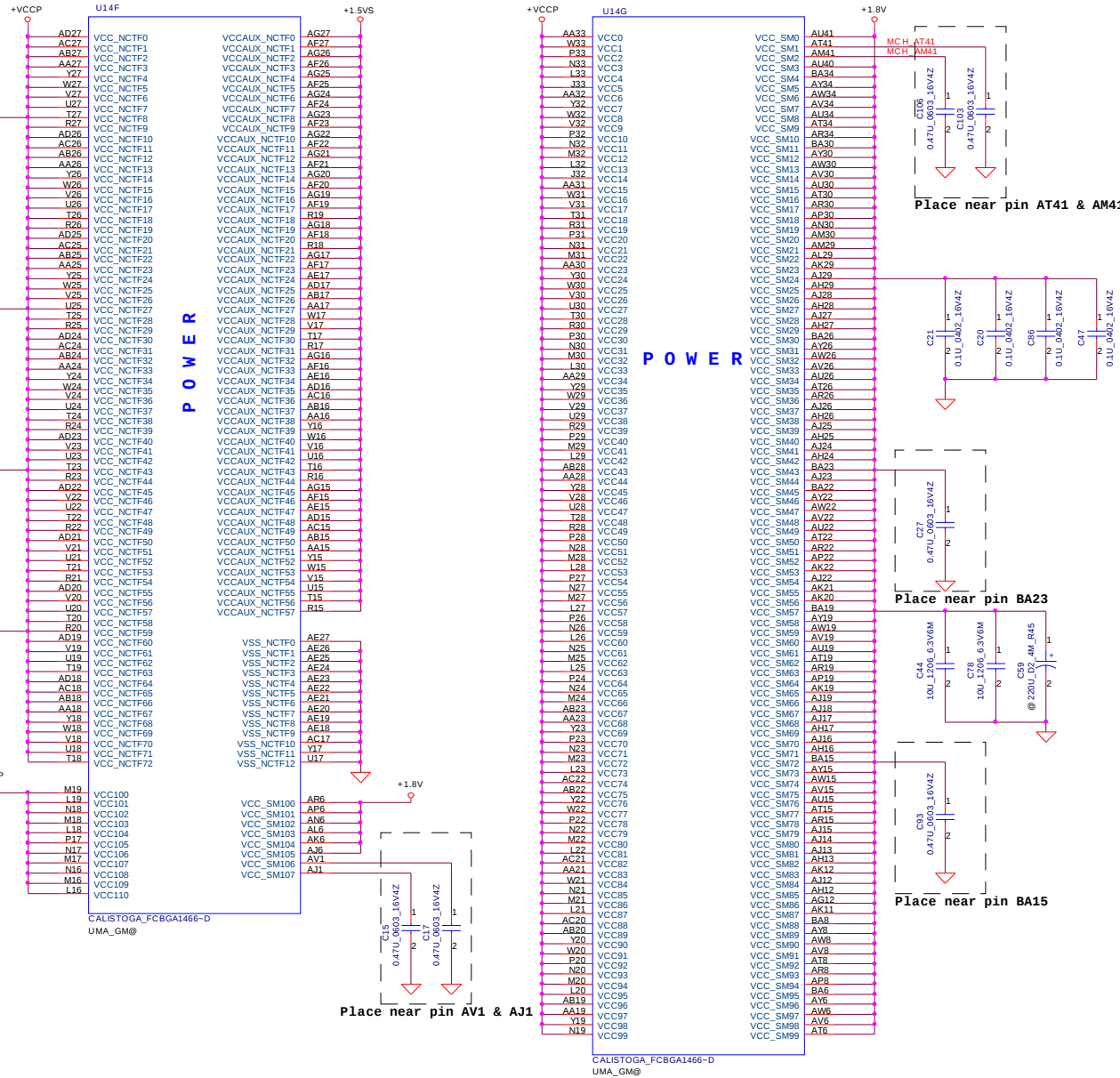
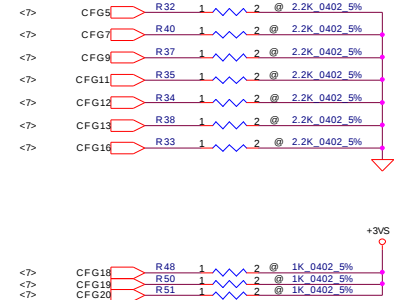


Strap Pin Table

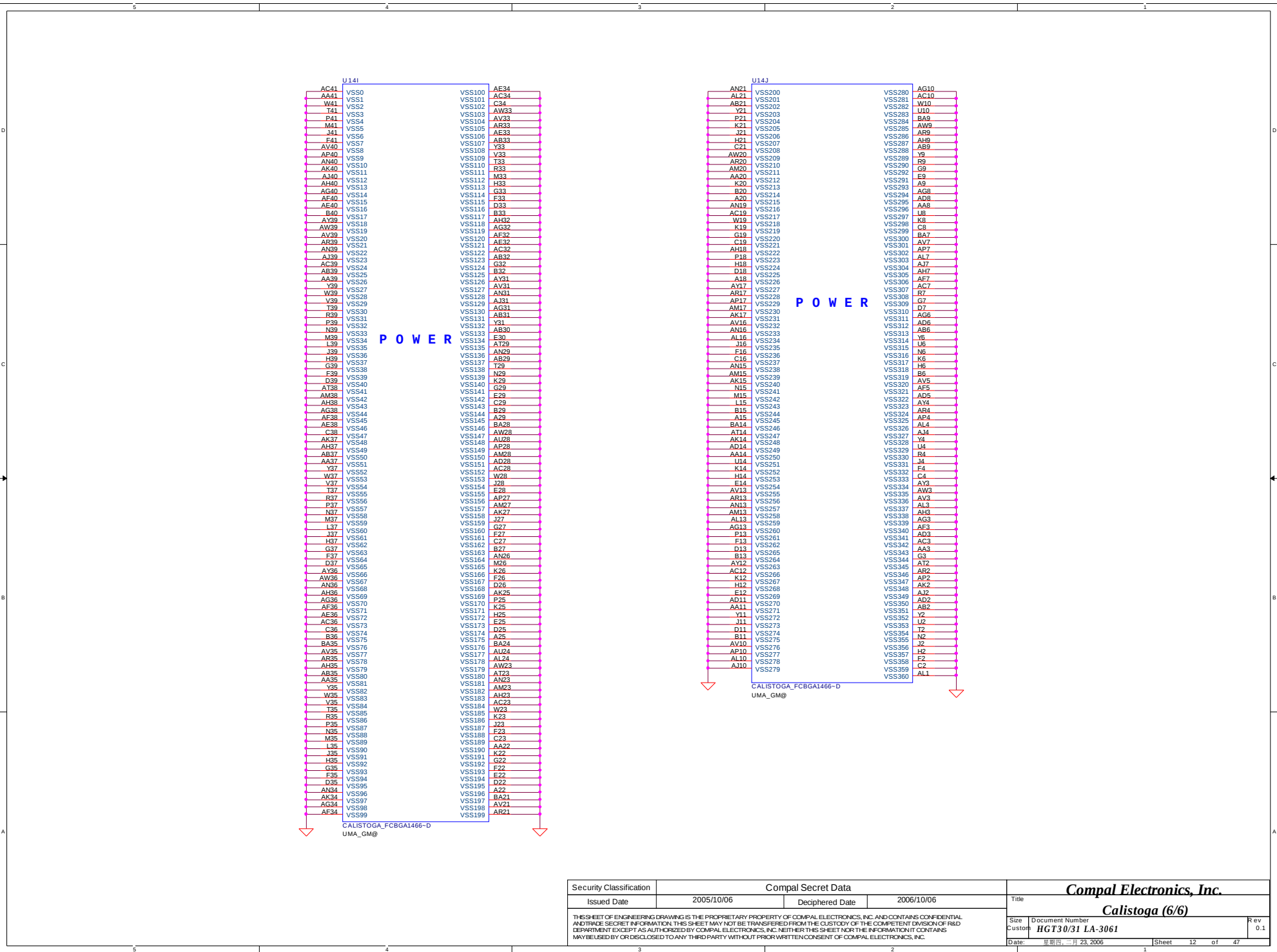
CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

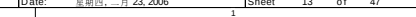
CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default) *
CFG66	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG10 CFG18	10 = 1.05V* (Default) 01 = 1.5V
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal * (Default)
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. * (Default) 1 = PCIe/SDVO are operating simu.

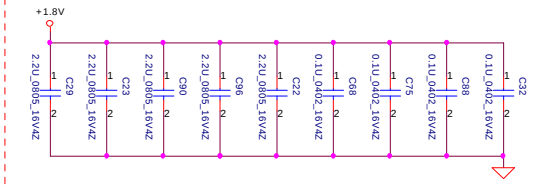
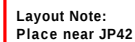


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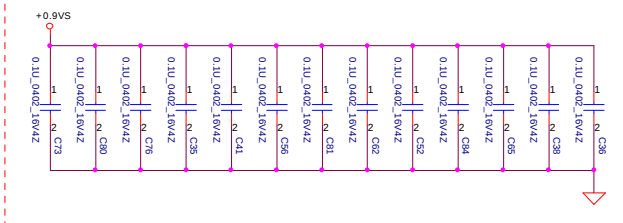


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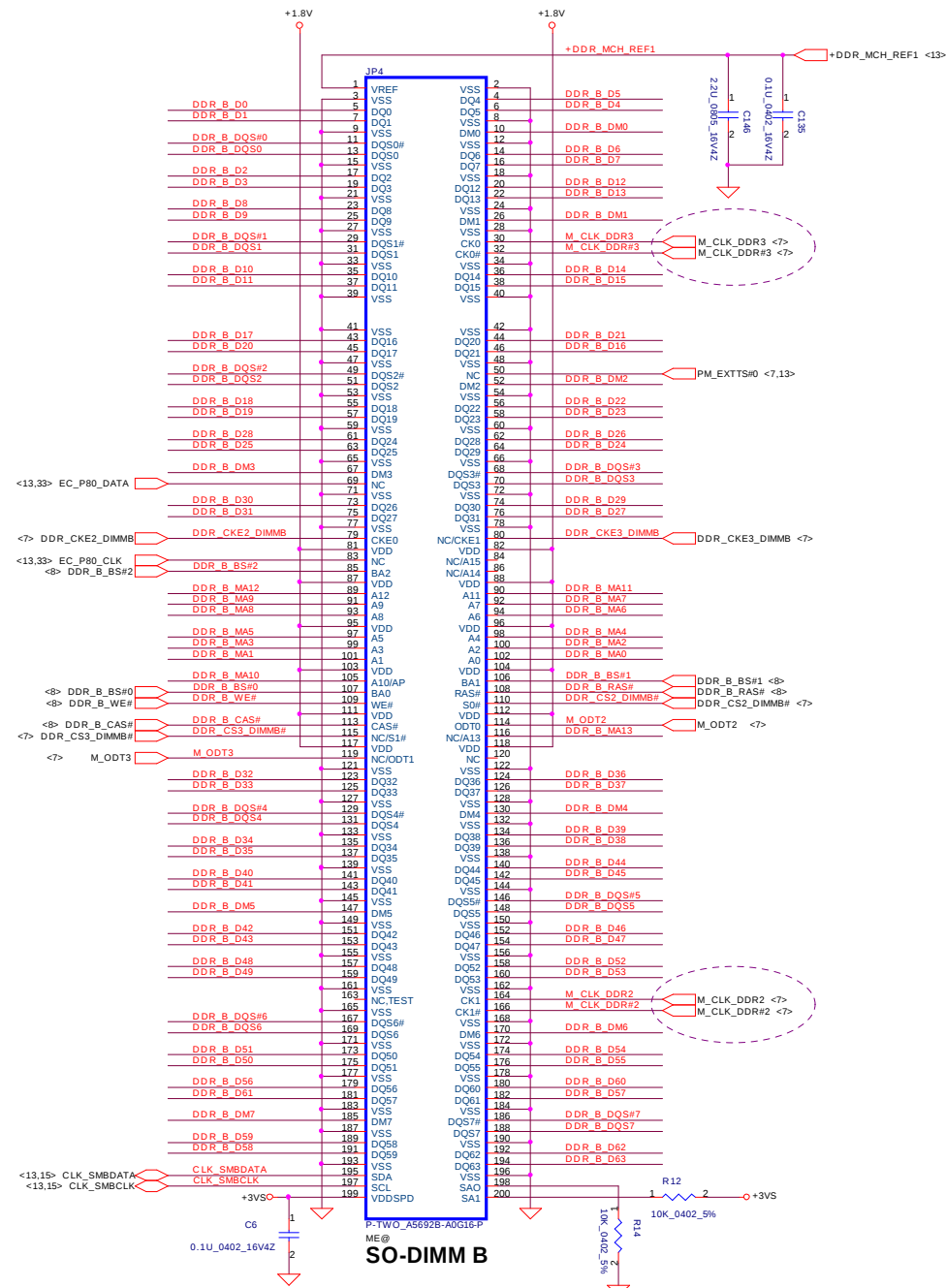
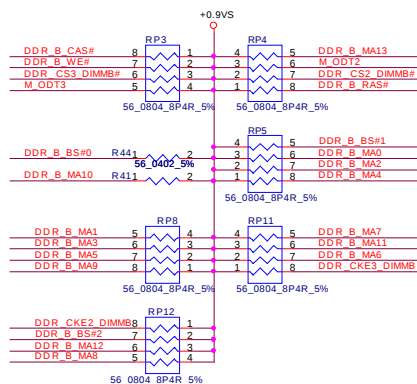




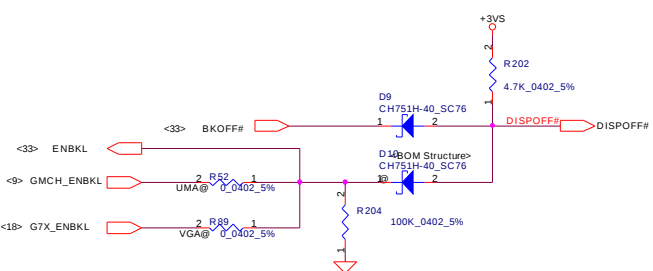
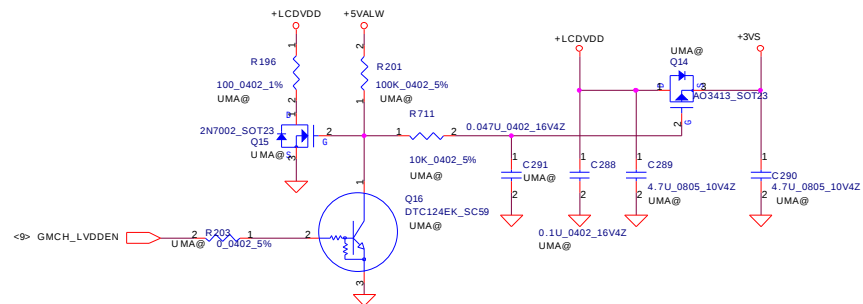
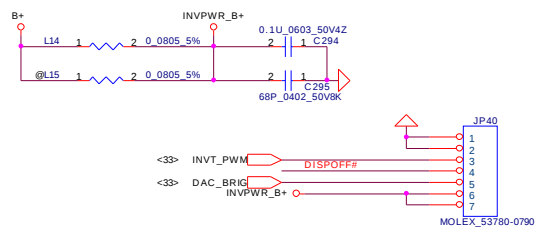
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor
closely JP42,all
trace length Max=1.5"

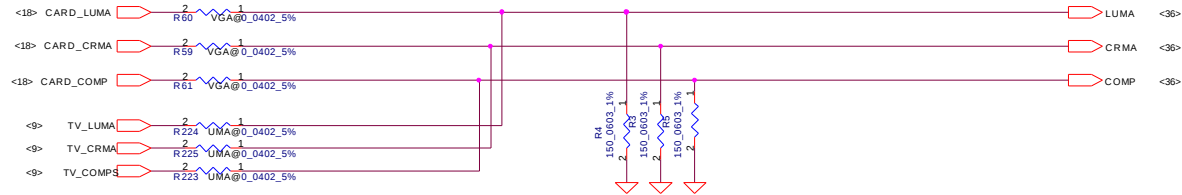


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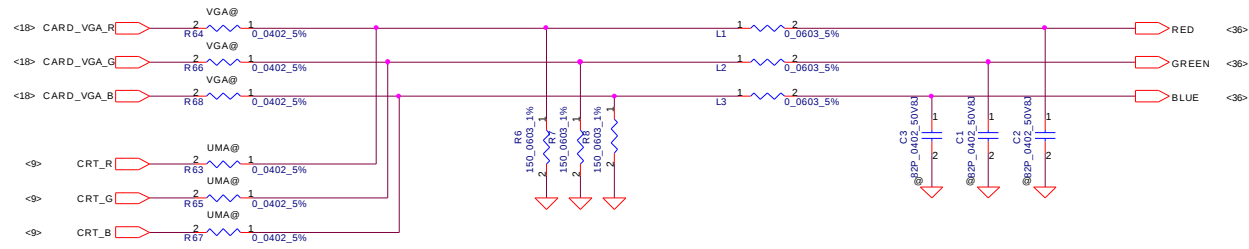


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Title		LVDS Connector			
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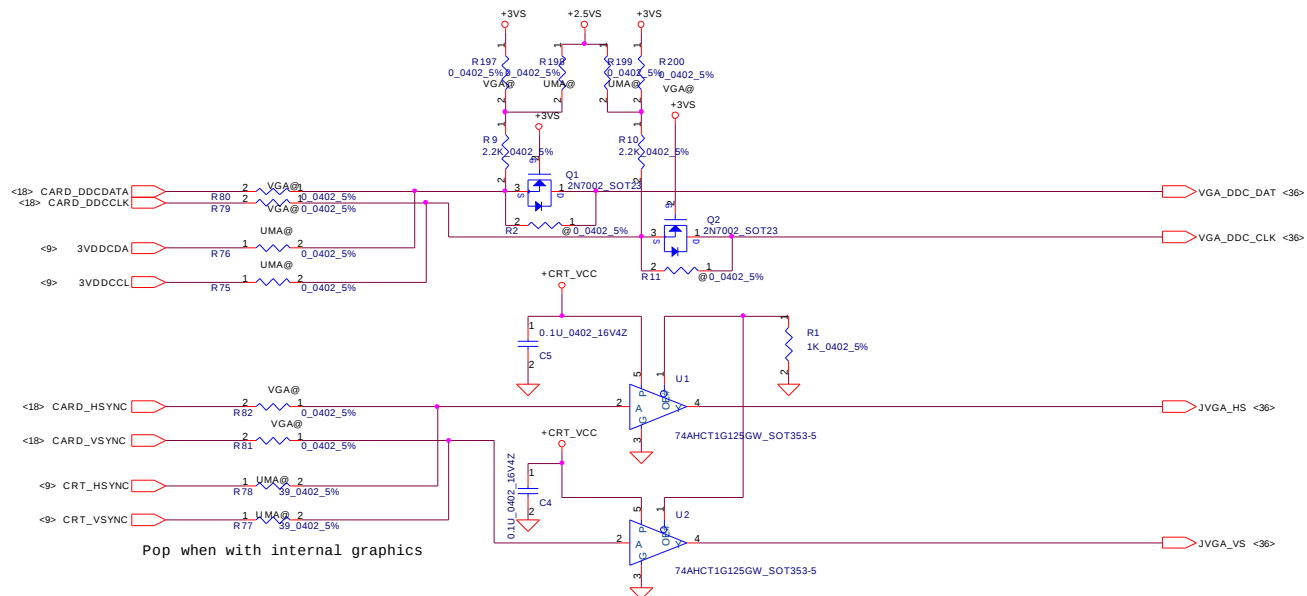
TV-OUT Conn.



Pop when with internal graphics

CRT Conn.

Pop when with internal graphics



Pop when with internal graphics

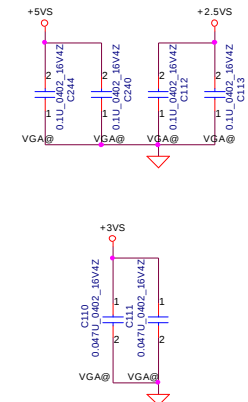
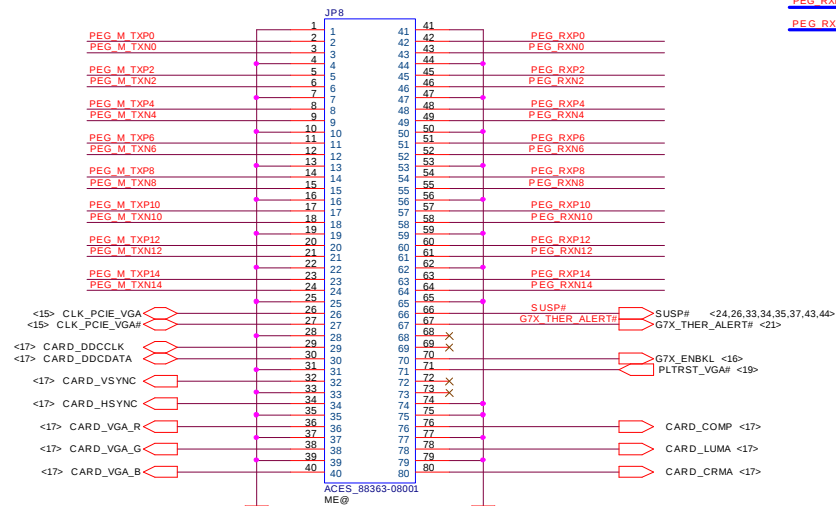
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MAX. 4.06A @ 1.8V
MAX. 130mA @ 2.5V
MAX. 655mA @ 3.3V

PEG_M_TXP[0..15] PEG_M_TXN[0..15] <9>
PEG_M_TXN[0..15] PEG_M_TXN[0..15] <9>
PEG_RXP[0..15] PEG_RXP[0..15] <9>
PEG_RXN[0..15] PEG_RXN[0..15] <9>



< New Add Pin.28 for +3VS, Pin.68 for +1.8VS @R03 >

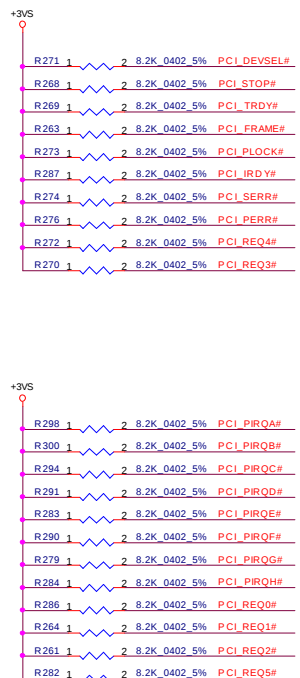


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VGA/B connector

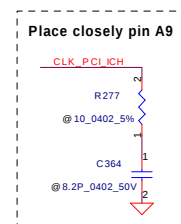
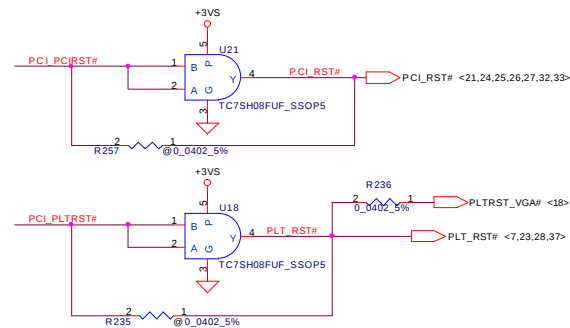
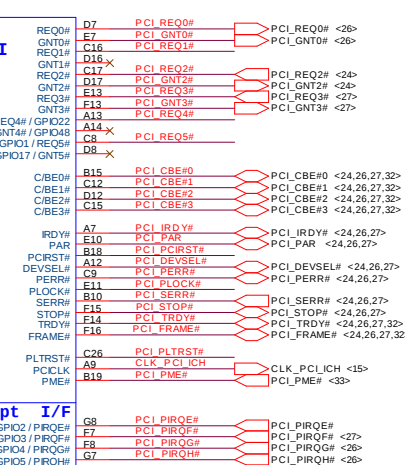
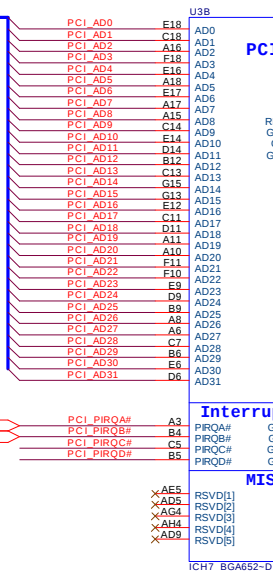
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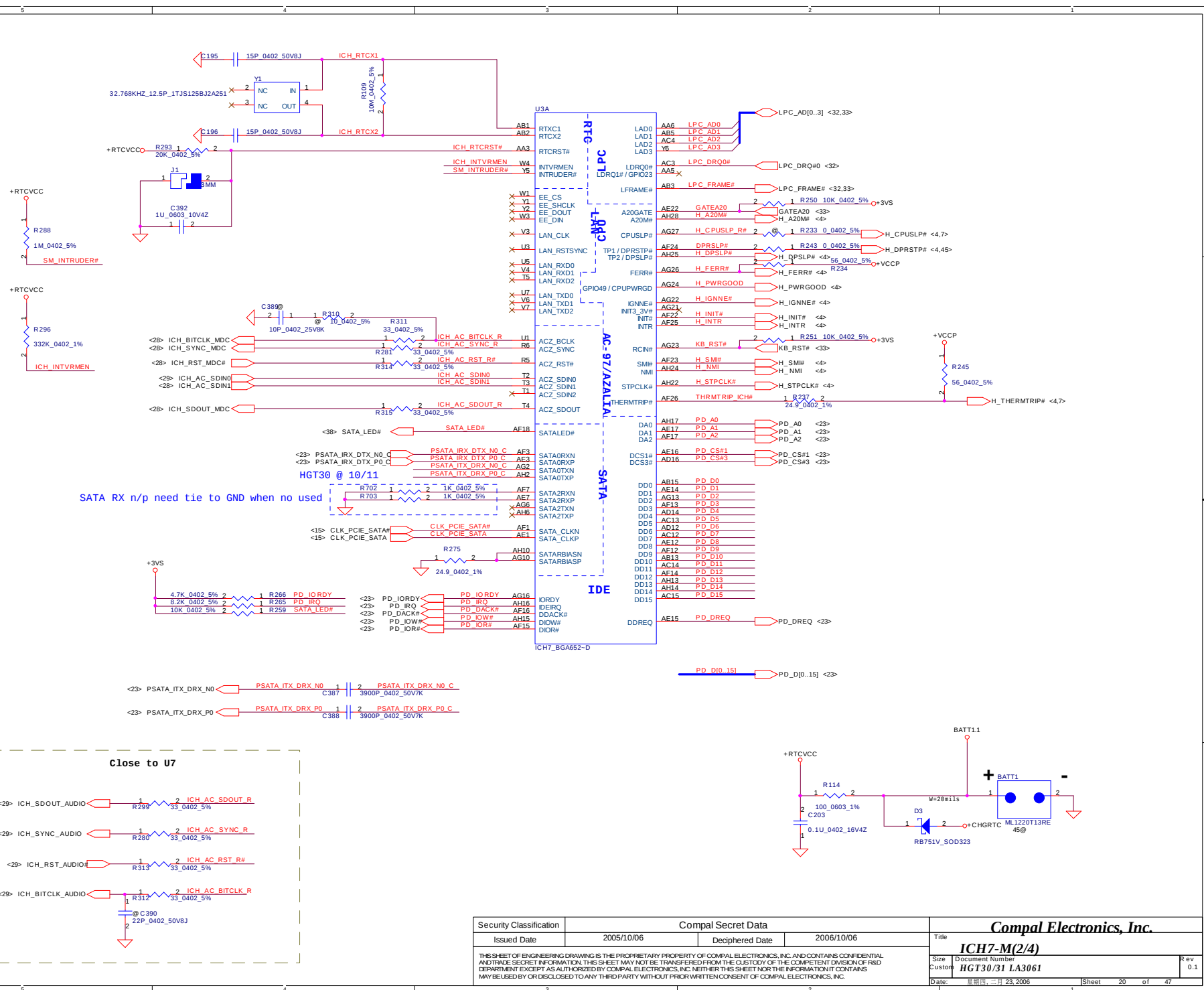


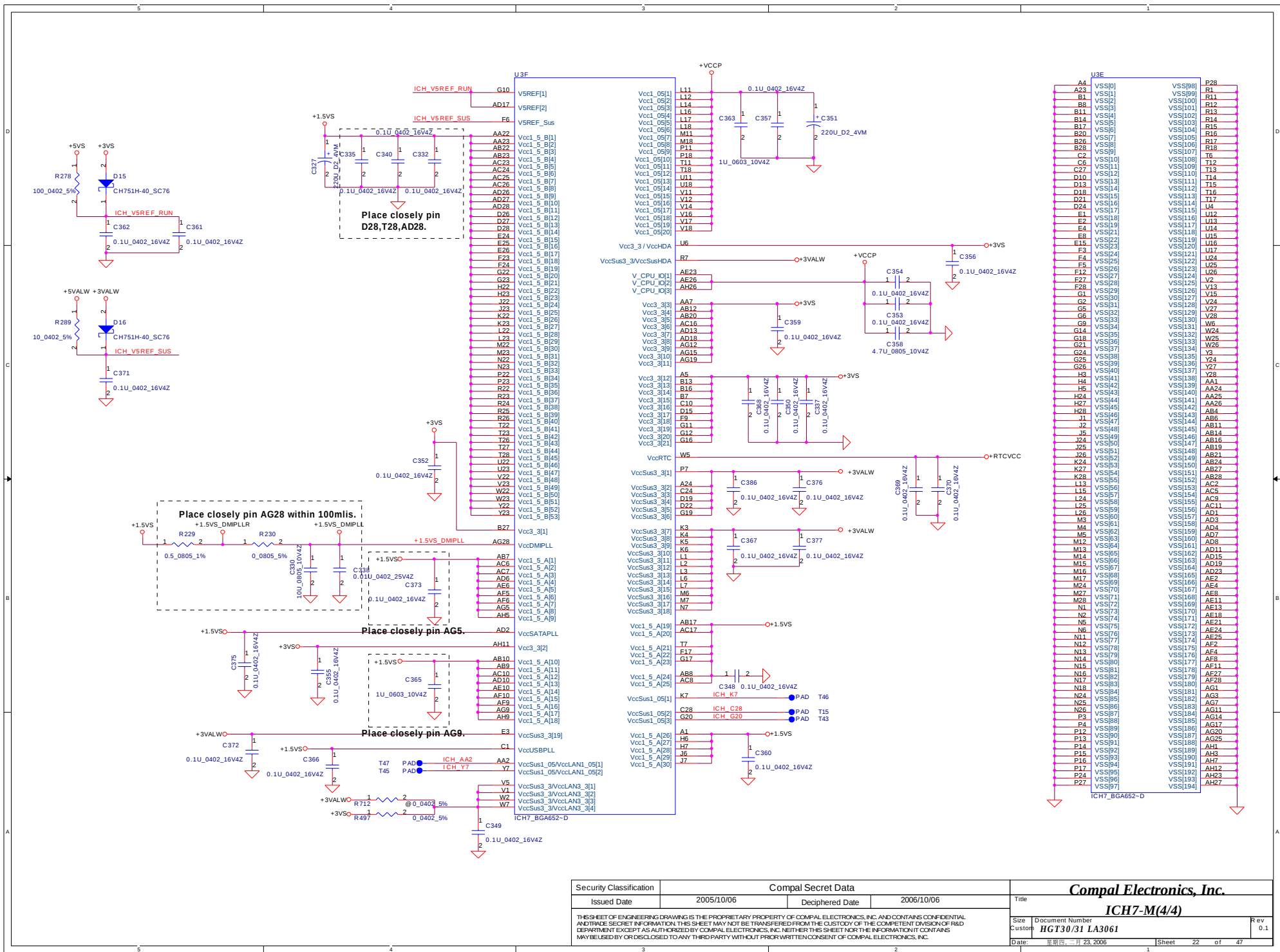
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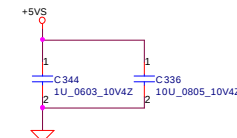
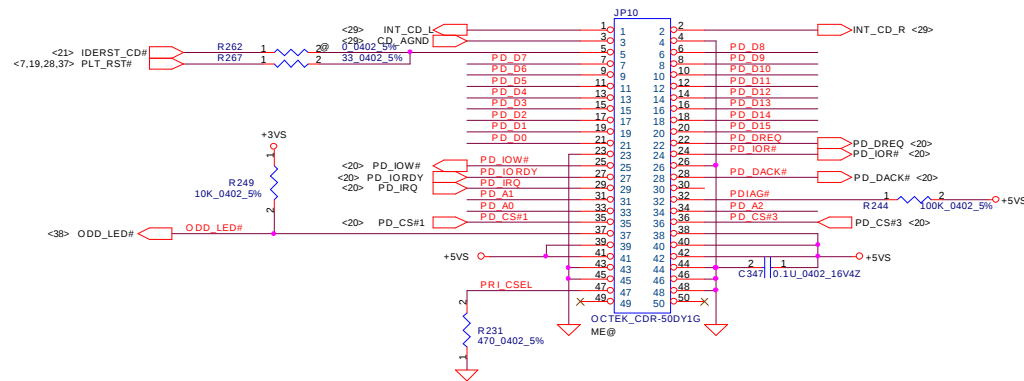
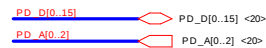
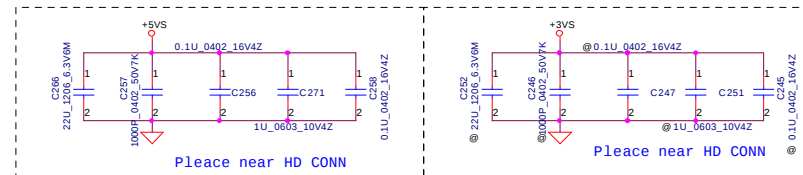
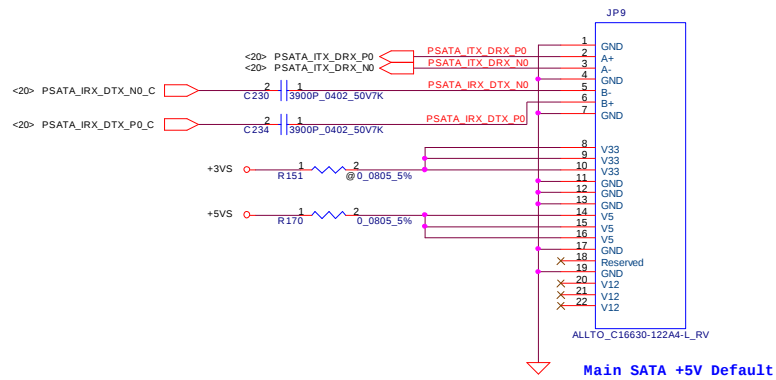
<24> PCI_PIRQA#
PCI_PIRQB#



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					ICH7-M(1/4)
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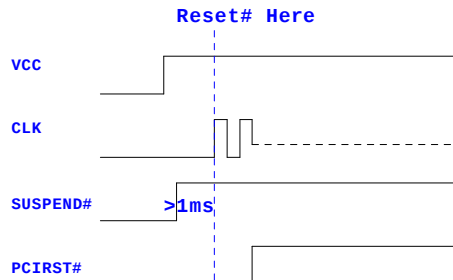




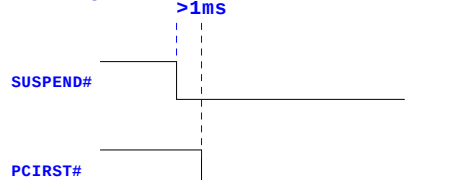


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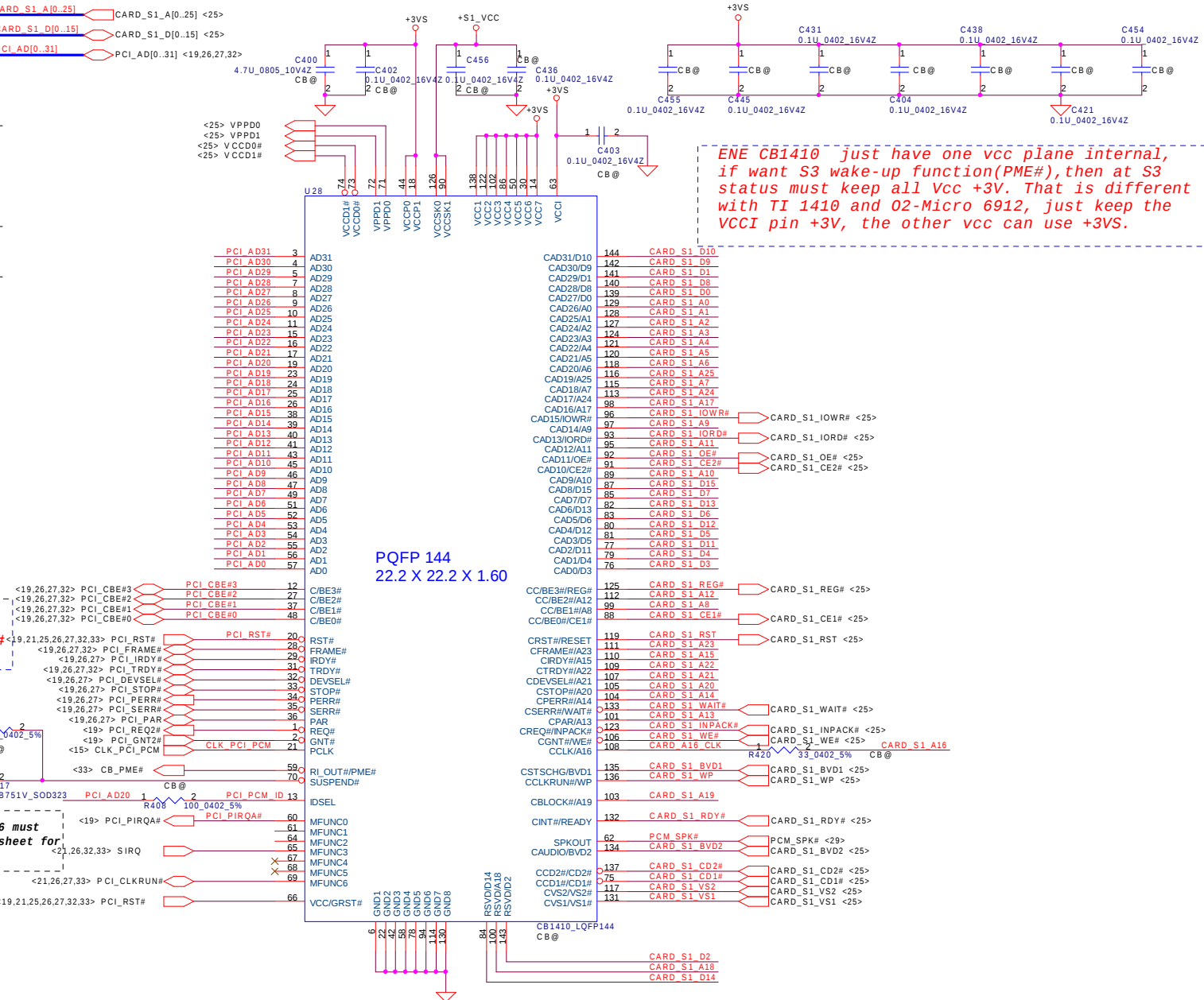
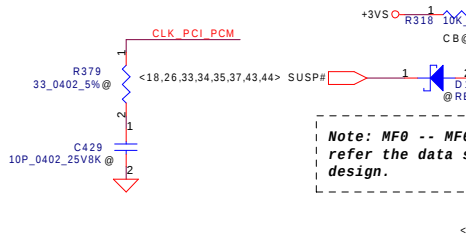
Power on RESET#



Entry S3



SUSPEND# will gate the PCIRST# or GRST#, so need S3 wake up function, SUSPEND# must be LOW ahead the PCIRST# about 1ms.



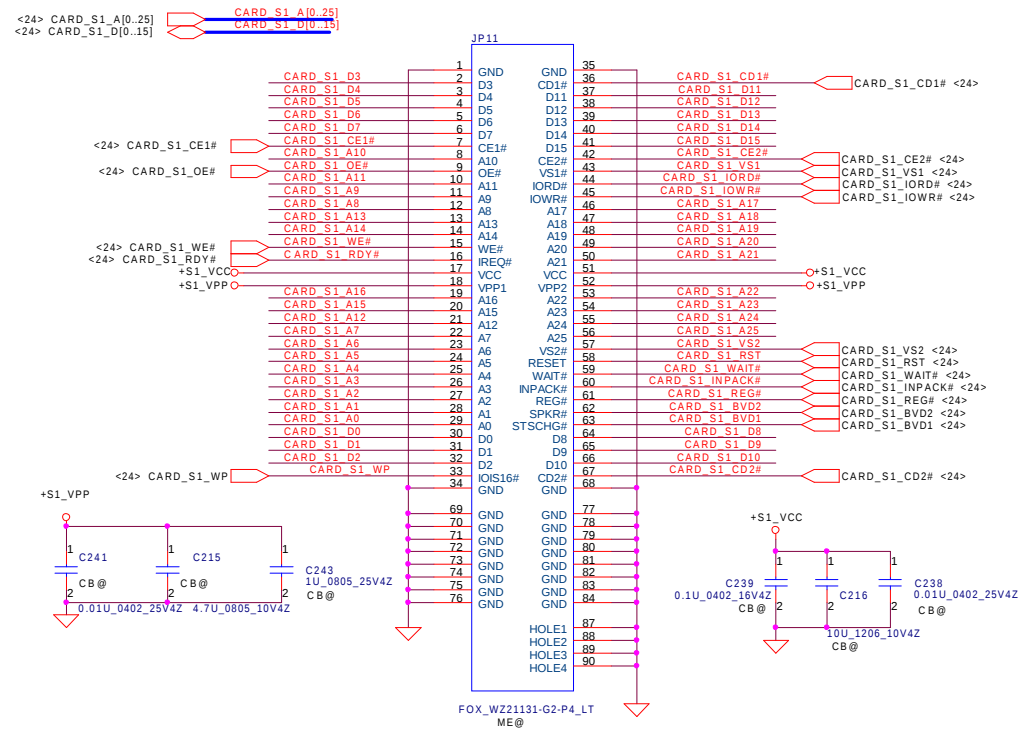
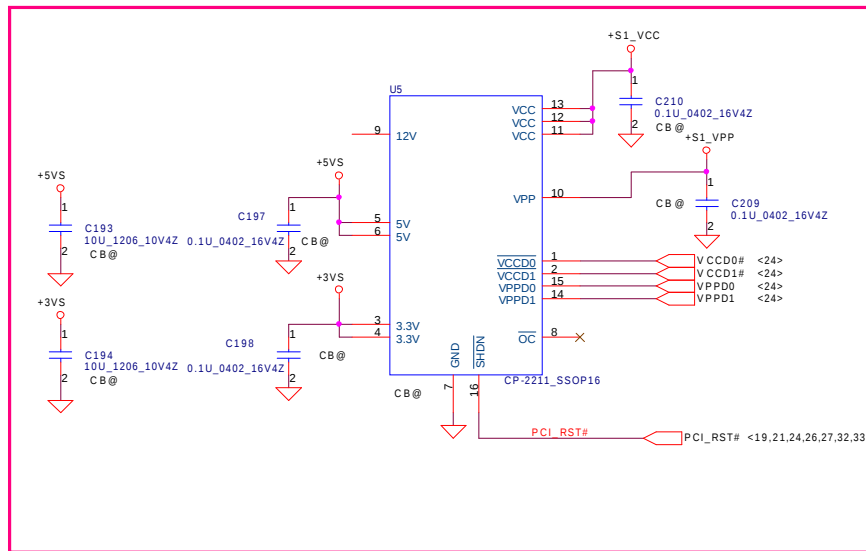
ENE CB1410 just have one vcc plane internal, if want S3 wake-up function(PME#), then at S3 status must keep all Vcc +3V. That is different with TI 1410 and 02-Micro 6912, just keep the VCCI pin +3V, the other vcc can use +3VS.

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2005/10/06		2006/10/06		CB ENE1410(One Solt)	
2005/10/06		2006/10/06		Size	Document Number
2005/10/06		2006/10/06		Custom	HGT30/31 LA3061
2005/10/06		2006/10/06		Date	Rev
2005/10/06		2006/10/06		2005/10/23	0.1

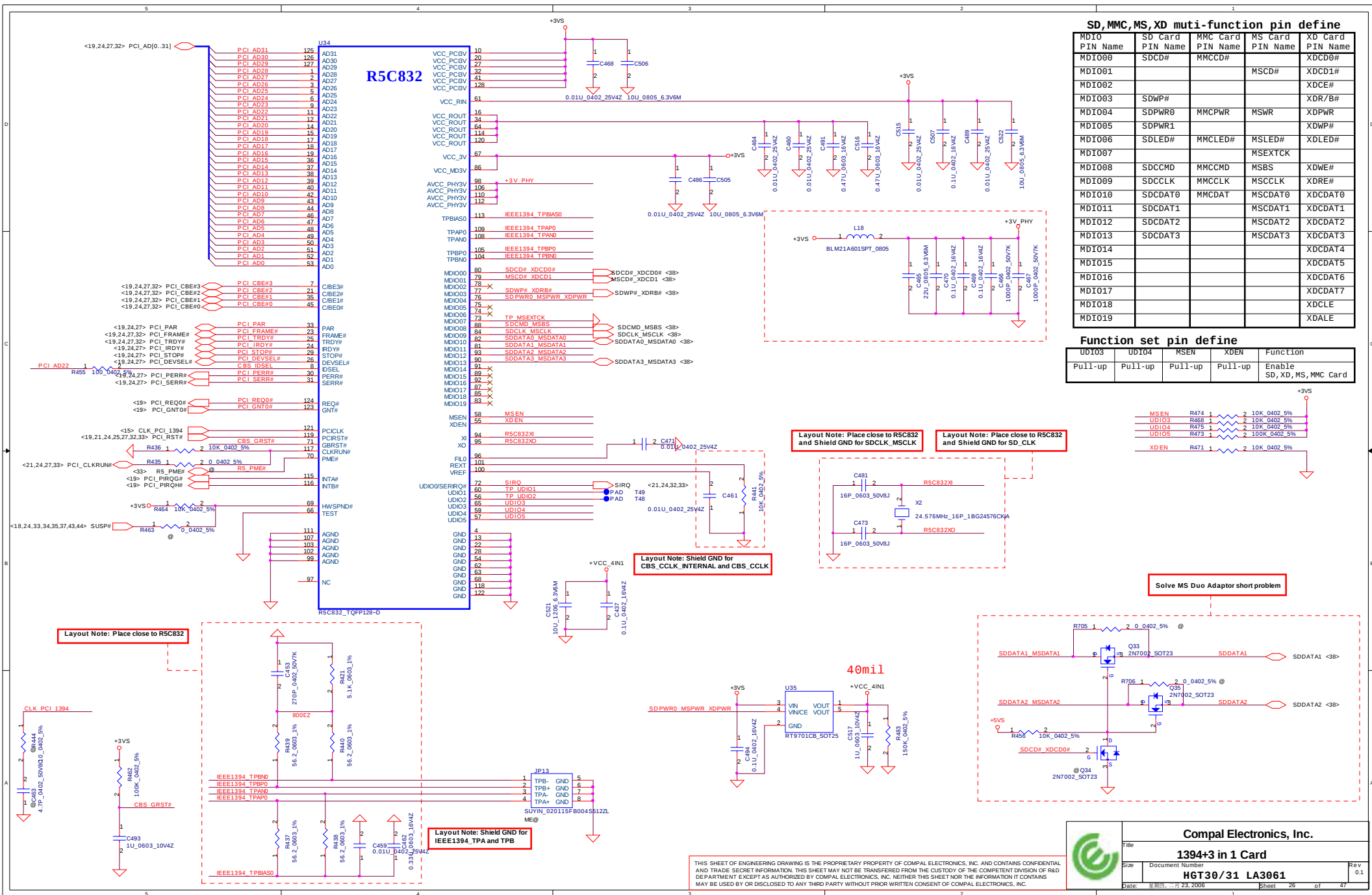
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PCMCIA Power Controller

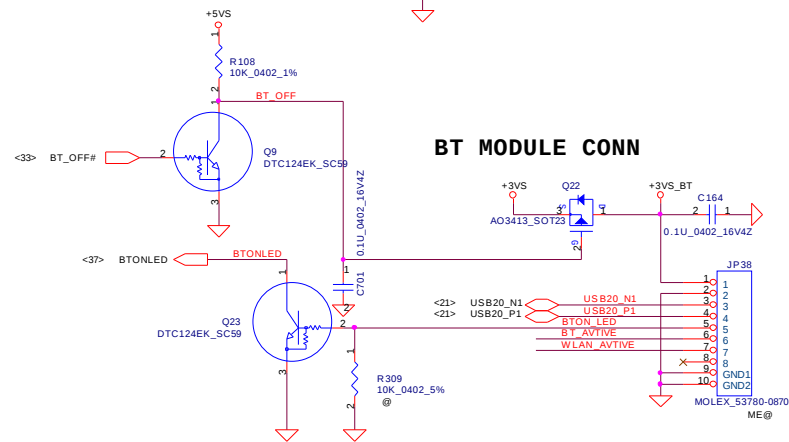
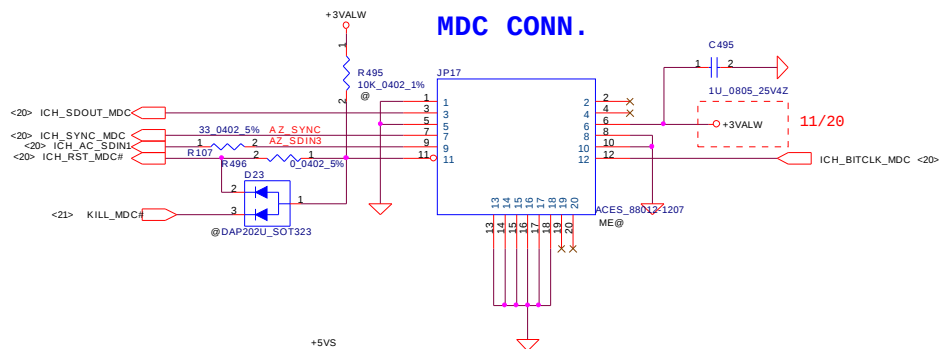


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Issued Date	2005/10/06	Deciphered Date	2006/10/06	Title	
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Size		Document Number		Rev	
Customer		HGT30/31 LA3061		0.1	
Date		星期四, 五月 23, 2006		Sheet 25 of 47	

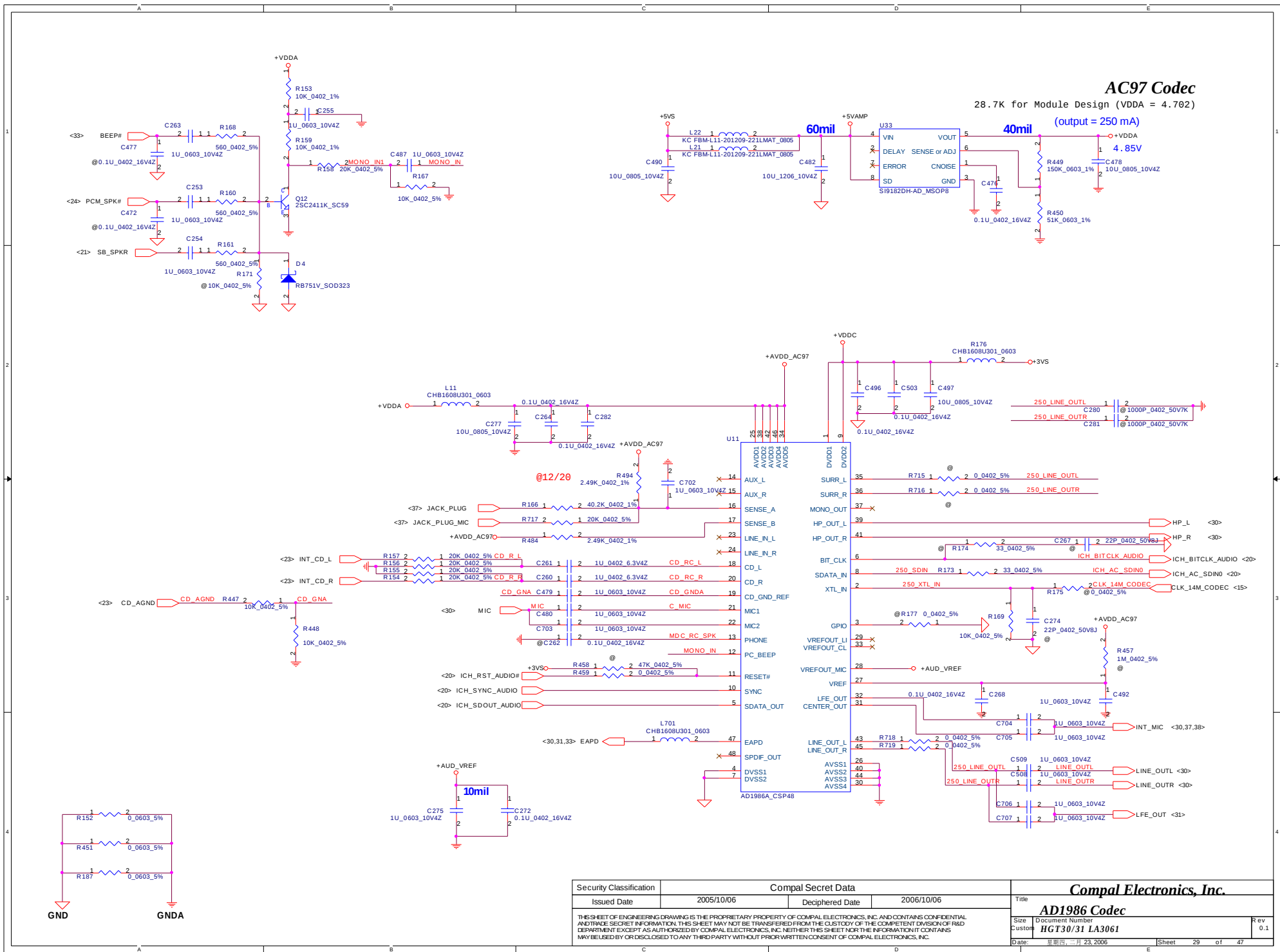


Pin-to-pin connection diagram for the FOX_A508-226-S56N-7F module. The diagram shows two columns of pins: JP16 on the left and GND1 on the right. Various signals are connected between these pins, including ICH_PCIE_WAKE#, BT_AVTTVE, WLAN_AVTTVE, CLKREQ_MCARD#, CLK_PCIE_MCARD#, CLK_PCIE_MCARDI, CLK_PCIE_MCARD, PCIE_RXN2, PCIE_RXP2, PCIE_TXN2, PCIE_TXP2, PLT_RST#, WL_OFF#, PLT_RST#, ICH_SMBCLK, ICH_SMBDATA, WIRELESS_LED#, and WIRELESS_LED#. Power pins are connected to +3VS and +1.5VS. The diagram also includes a table of pin numbers and their corresponding connections.

Signal	Pin	Signal	Pin
ICH_PCIE_WAKE#	1	2	2
BT_AVTTVE	2	3	3
WLAN_AVTTVE	3	4	4
CLKREQ_MCARD#	4	5	5
CLK_PCIE_MCARD#	5	6	6
CLK_PCIE_MCARDI	6	7	7
CLK_PCIE_MCARD	7	8	8
PCIE_RXN2	8	9	9
PCIE_RXP2	9	10	10
PCIE_TXN2	10	11	11
PCIE_TXP2	11	12	12
PLT_RST#	12	13	13
WL_OFF#	13	14	14
PLT_RST#	14	15	15
ICH_SMBCLK	15	16	16
ICH_SMBDATA	16	17	17
WIRELESS_LED#	17	18	18
WIRELESS_LED#	18	19	19
	19	20	20
	20	21	21
	21	22	22
	22	23	23
	23	24	24
	24	25	25
	25	26	26
	26	27	27
	27	28	28
	28	29	29
	29	30	30
	30	31	31
	31	32	32
	32	33	33
	33	34	34
	34	35	35
	35	36	36
	36	37	37
	37	38	38
	38	39	39
	39	40	40
	40	41	41
	41	42	42
	42	43	43
	43	44	44
	44	45	45
	45	46	46
	46	47	47
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	51	52	52
	52	53	53
	53	54	54

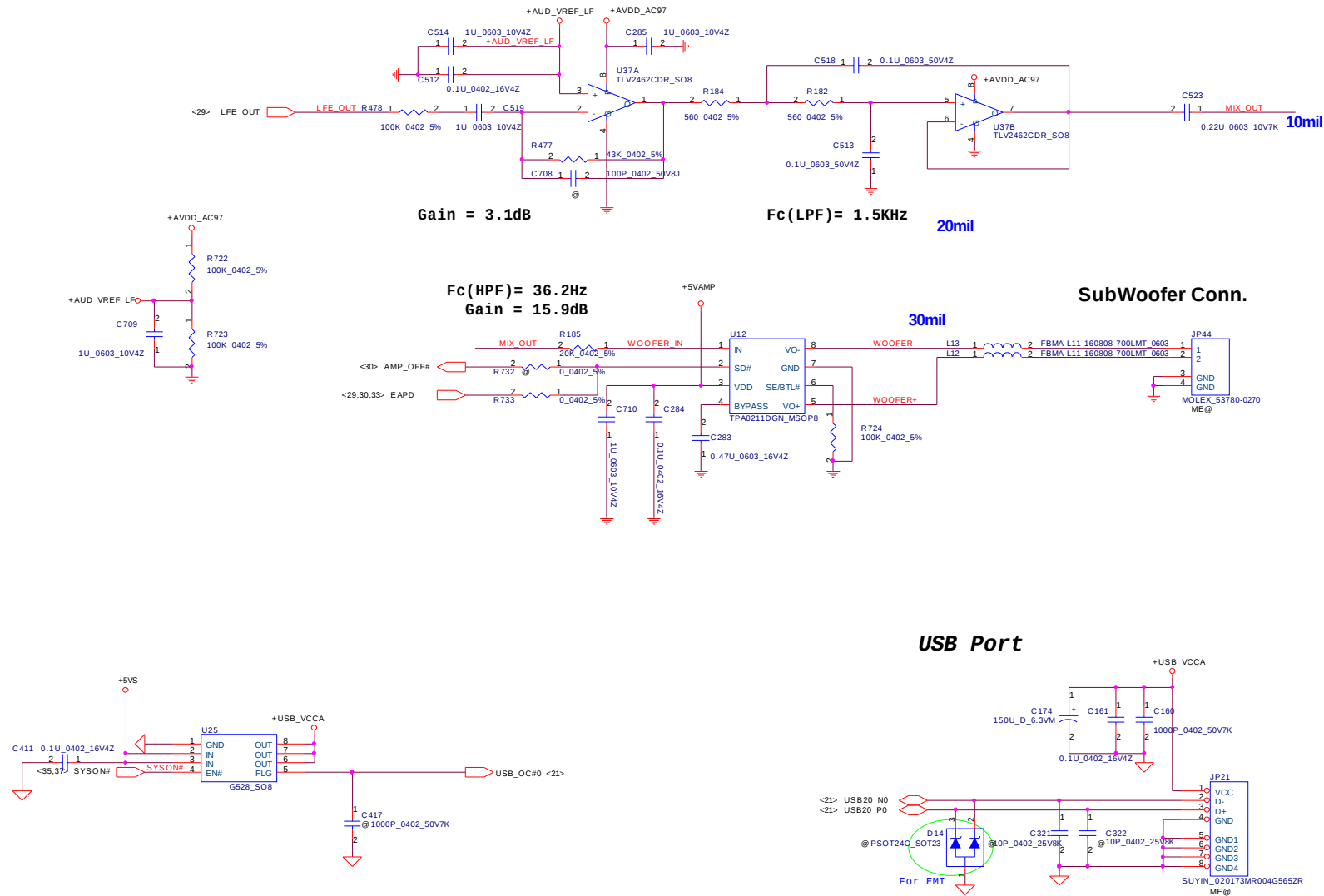


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				Date: 星期五, 二月 23, 2006	Sheet 28 of 47



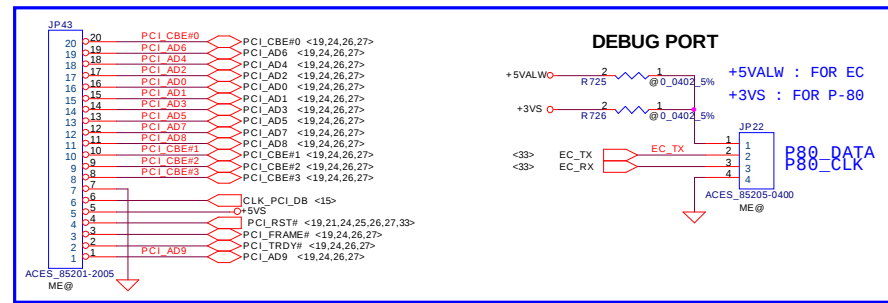
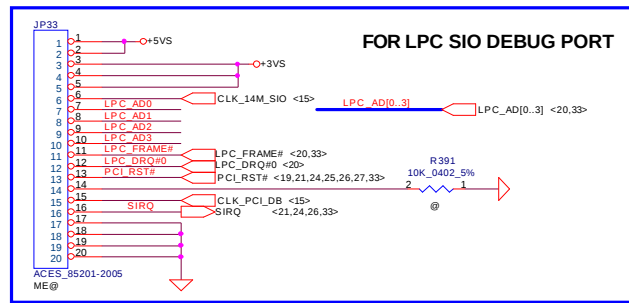
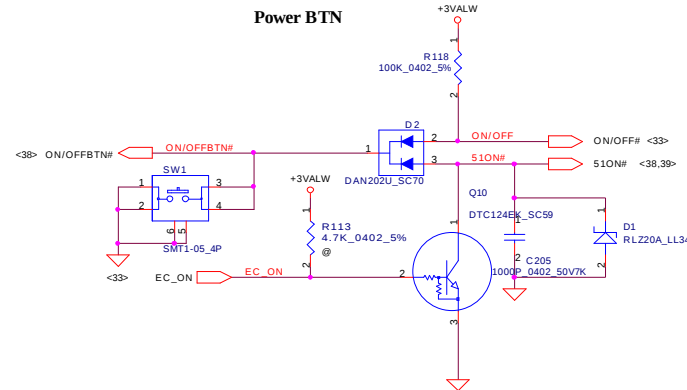
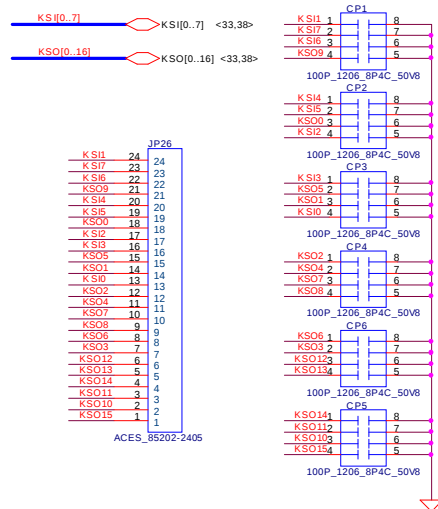
SUBWOOFER (Reserved for C38)

WOOFER@

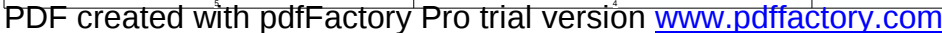


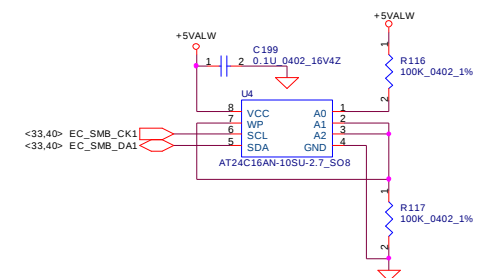
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Issued Date	2005/10/06	Deciphered Date	2006/10/06	Bluetooth & USB CONN.
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				Rev 0.1
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INT_KBD CONN.(TYPE "D" KB)



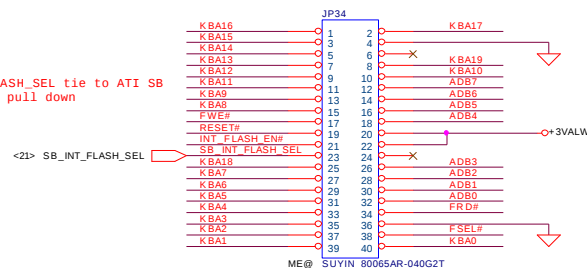
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Size	Document Number	KBD_ON/OFF,T/P,LED/B,DEBUG		Rev
Custom	HGT30/31 LA3061			0.1
Date:	星期五, 二月 23, 2006	Sheet	32	of 47



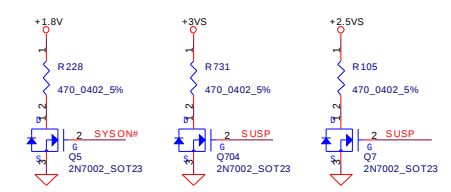
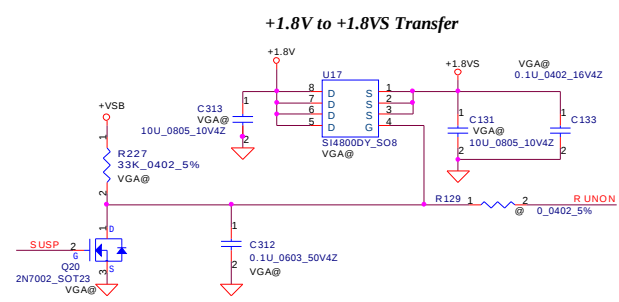
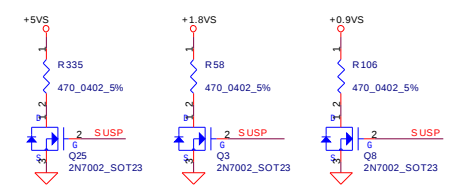
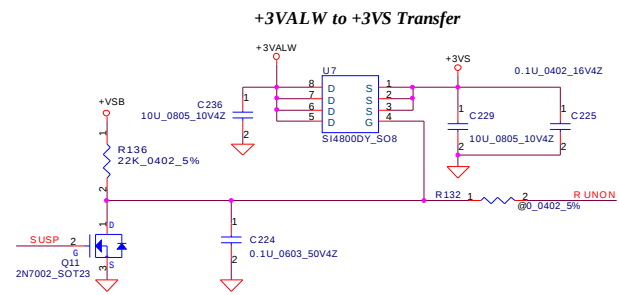
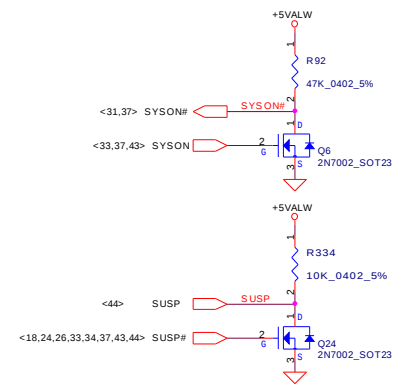
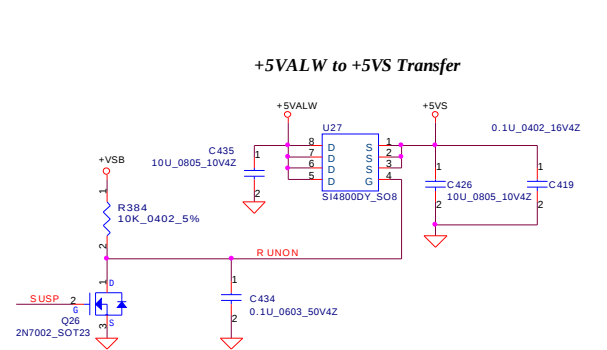


Pin connection diagram for the SST39VF080-70-4C-E1E_TSP40. The diagram shows a 40-pin package with pins 1-20 on the left and 21-40 on the right. Pin 1 is connected to KBA0, pin 2 to KBA1, and so on. Pin 20 is connected to INT_FSEL#. Pin 21 is connected to FRD#. Pin 22 is connected to FWE#. Pin 23 is connected to CE#. Pin 24 is connected to OE#. Pin 25 is connected to WE#. Pin 26 is connected to GND0. Pin 27 is connected to GND1. Pin 28 is connected to GND2. Pin 29 is connected to GND3. Pin 30 is connected to GND4. Pin 31 is connected to GND5. Pin 32 is connected to GND6. Pin 33 is connected to GND7. Pin 34 is connected to GND8. Pin 35 is connected to GND9. Pin 36 is connected to GND10. Pin 37 is connected to GND11. Pin 38 is connected to GND12. Pin 39 is connected to GND13. Pin 40 is connected to GND14. The diagram also shows a 3V3VALW supply connected to pin 31 and a 0.1µF capacitor connected to pins 31 and 32. A 10K resistor is connected to pins 11 and 12. A 100K resistor is connected to pins 12 and 13. A 3V3VALW supply is connected to pin 11. A 3V3VALW supply is connected to pin 12. A 3V3VALW supply is connected to pin 13. A 3V3VALW supply is connected to pin 14. A 3V3VALW supply is connected to pin 15. A 3V3VALW supply is connected to pin 16. A 3V3VALW supply is connected to pin 17. A 3V3VALW supply is connected to pin 18. A 3V3VALW supply is connected to pin 19. A 3V3VALW supply is connected to pin 20. A 3V3VALW supply is connected to pin 21. A 3V3VALW supply is connected to pin 22. A 3V3VALW supply is connected to pin 23. A 3V3VALW supply is connected to pin 24. A 3V3VALW supply is connected to pin 25. A 3V3VALW supply is connected to pin 26. A 3V3VALW supply is connected to pin 27. A 3V3VALW supply is connected to pin 28. A 3V3VALW supply is connected to pin 29. A 3V3VALW supply is connected to pin 30. A 3V3VALW supply is connected to pin 31. A 3V3VALW supply is connected to pin 32. A 3V3VALW supply is connected to pin 33. A 3V3VALW supply is connected to pin 34. A 3V3VALW supply is connected to pin 35. A 3V3VALW supply is connected to pin 36. A 3V3VALW supply is connected to pin 37. A 3V3VALW supply is connected to pin 38. A 3V3VALW supply is connected to pin 39. A 3V3VALW supply is connected to pin 40.

SB_INT_FLASH_SEL tie to ATI SB
GPIO1 and pull down

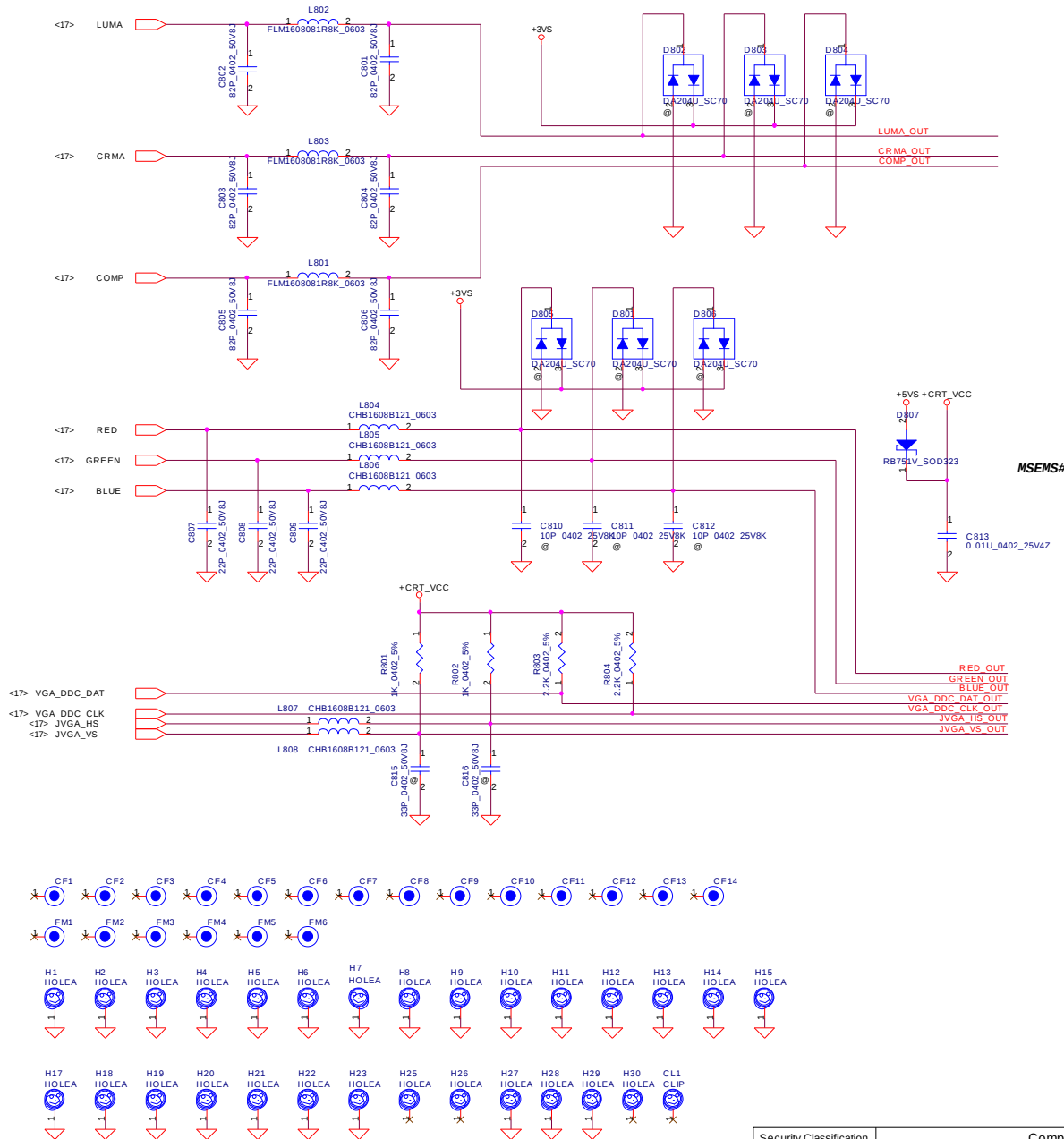


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				Date	星期五, 二月 23, 2006	I Sheet 34 of 47



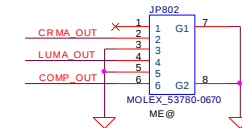
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/10/06	Deciphered Date	2006/10/06	Title
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				Size
				Custom
				Date
				Sheet
				of
				47
				Rev
				0.1

CLOSE TO JTVOUT1

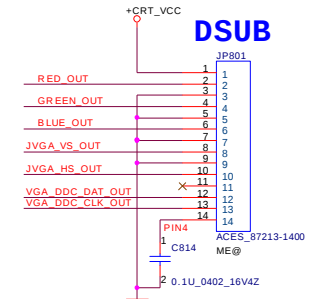


VGA I/O PORT Connector

S-VIDEO



DSUB



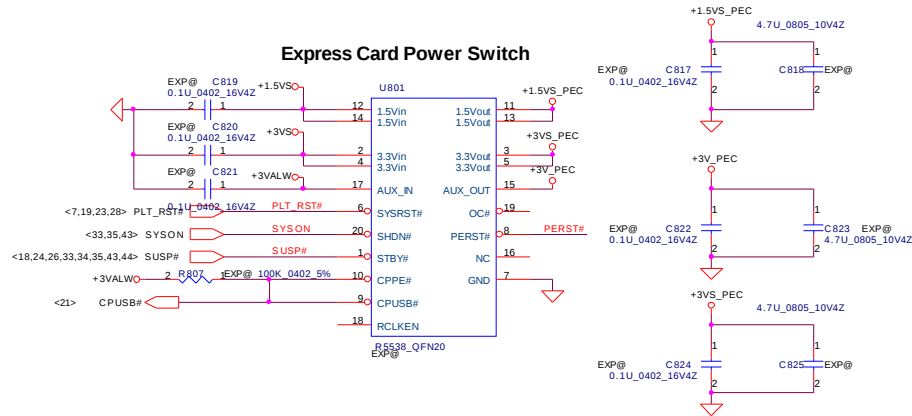
PIN ASSIGMENT

PIN	D-SUB	FUNCTION	PIN	SVIDEO	FUNCTION
1	9	+CRT_VCC	1	1	NC
2	1	RED	2	4	CRMA
3	6	GND	3	2	GND
4	2	GREEN	4	3	LUMA
5	7	GND	5	5	GND
6	3	BLUE	6	6	CVBS
7	8	GND			
8	14	VSYNC			
9	10	GND			
10	13	HSYNC			
11	11	SENSE			
12	12	SM_DAT			
13	15	SM_CLK			
14	4	PIN4			

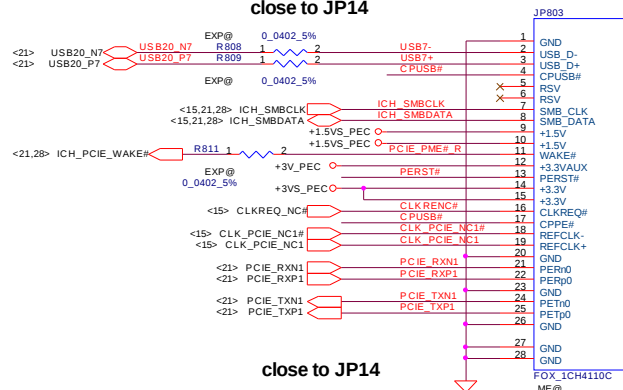
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				Size Document Number
				Custom HGT30/31 LA3061
				Rev 0.1
				Date: 2006/03/23
				Sheet 36 of 47

NEW CARD FOR C38

Express Card Power Switch

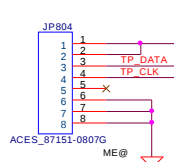


close to JP14

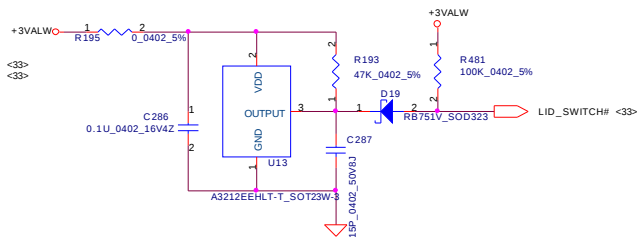


close to JP14

T/P Board



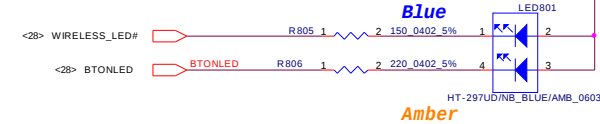
LID Switch



LED Indicator ON M/B

3 2 1
B B A B A

Wireless / Bluetooth LED

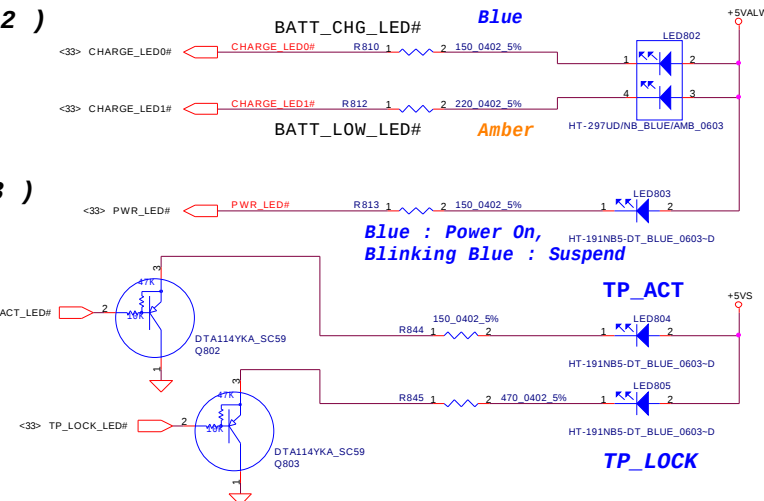


STATUS	
AC	BLUE
Chargin	Blinking Blue
Low BATT	Amber

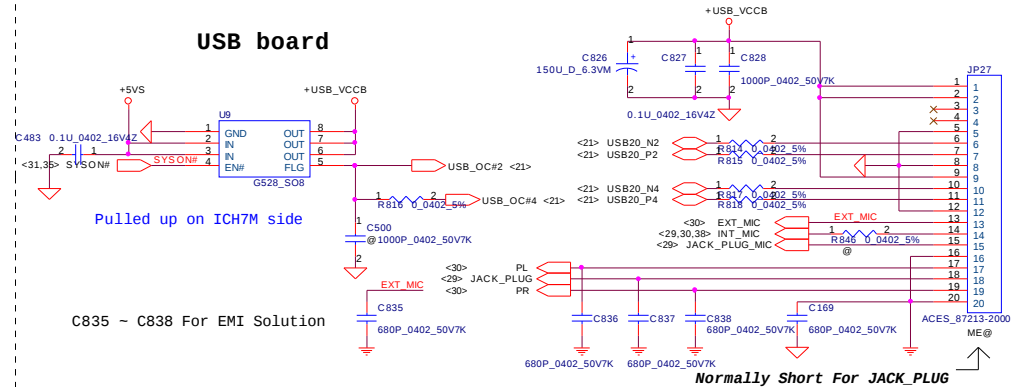
(1)

(2)

(3)



USB board



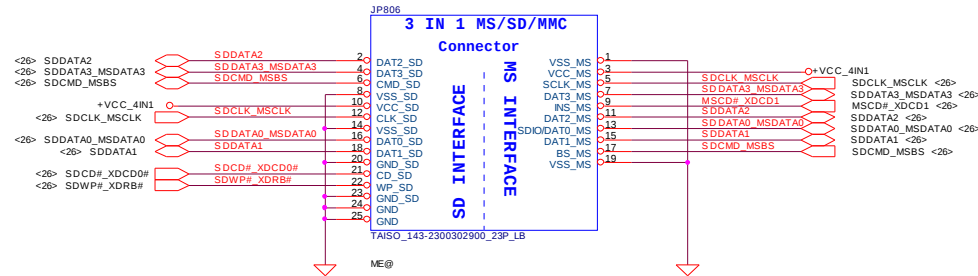
Pulled up on ICH7M side

C835 ~ C838 For EMI Solution

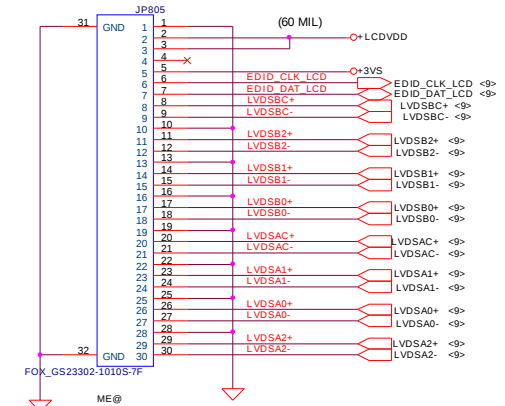
Normally Short For JACK_PLUG

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		Date	Rev 0.1
		Sheet	37 of 47

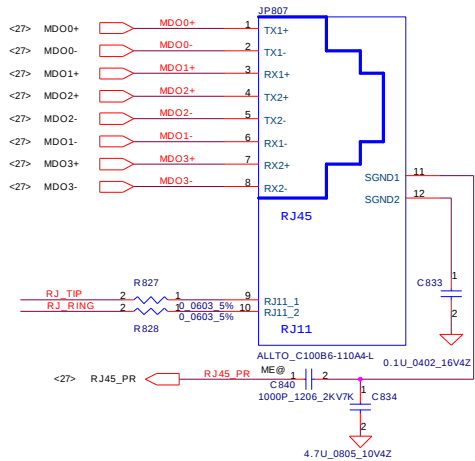
3 IN 1 Card Reader



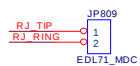
UMA LCD/PANEL Conn.



RJ11+RJ45 CONN

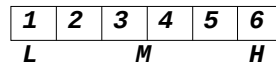


MDC CONN



SWITCH BD

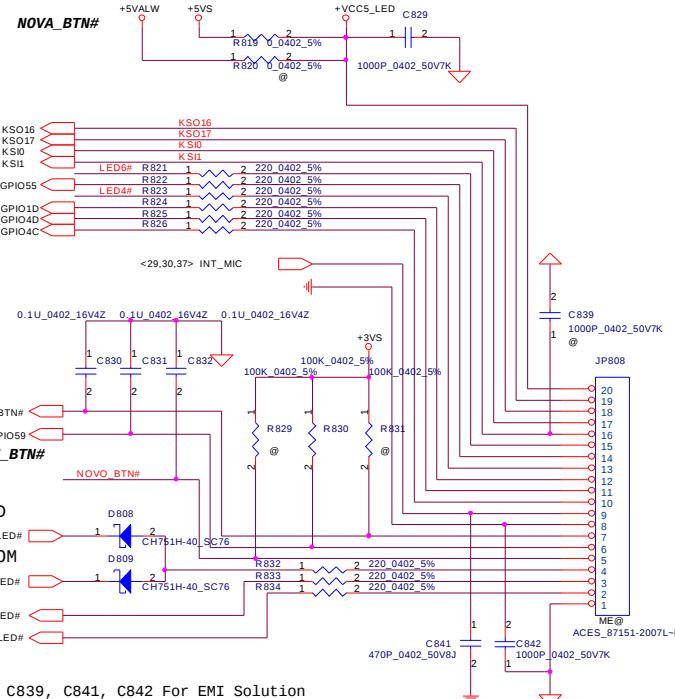
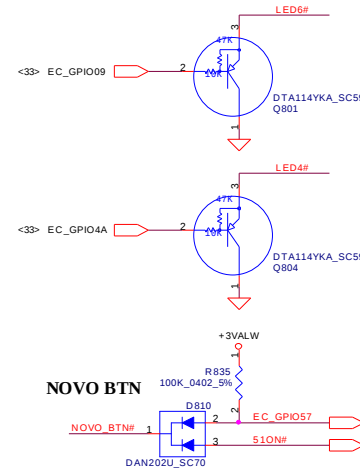
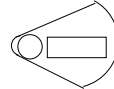
LED Indicator BD



Function

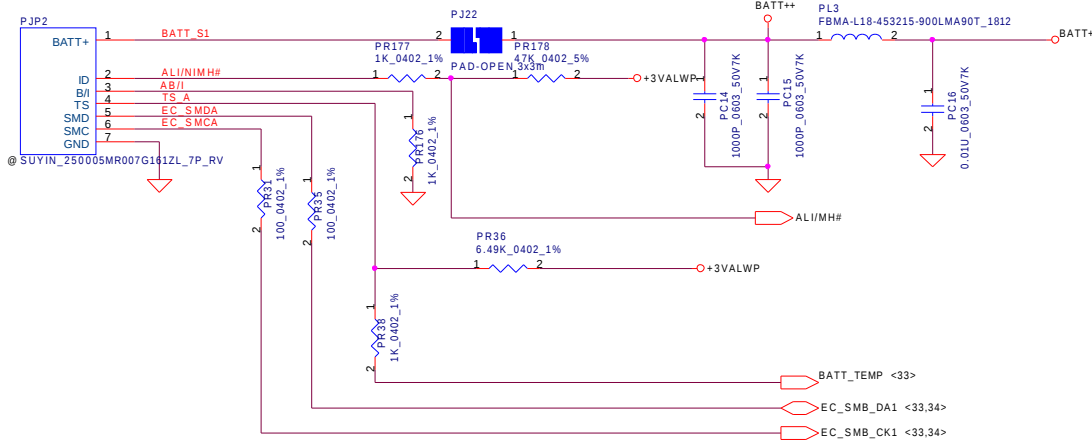
KEY Matrix	K016	K017
KS10	DW-UP	DW-DOWN
KS11	DW-ENTER	MUTE

Dial Wheel

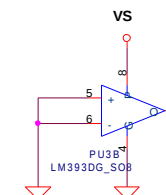
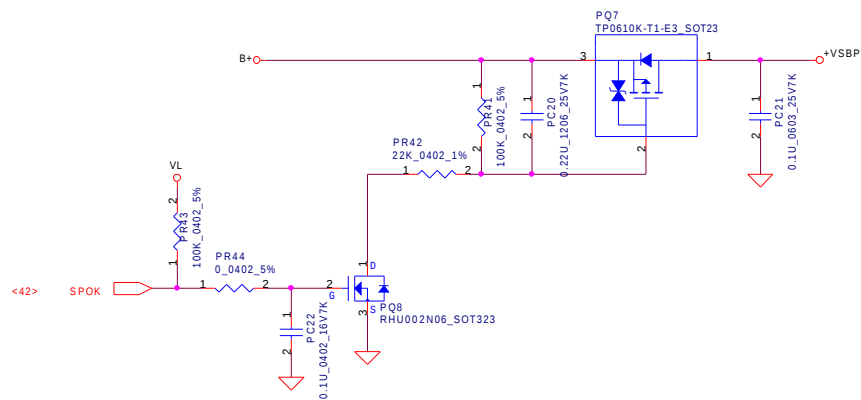
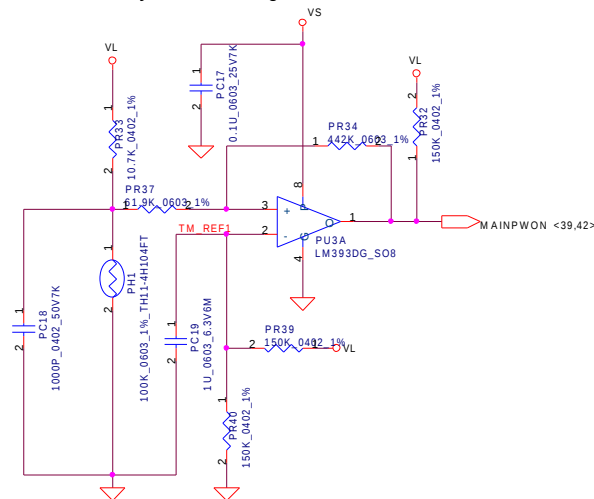


C839, C841, C842 For EMI Solution

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PH1 under CPU bottom side :
CPU thermal protection at 85 degree C
Recovery at 70 degree C

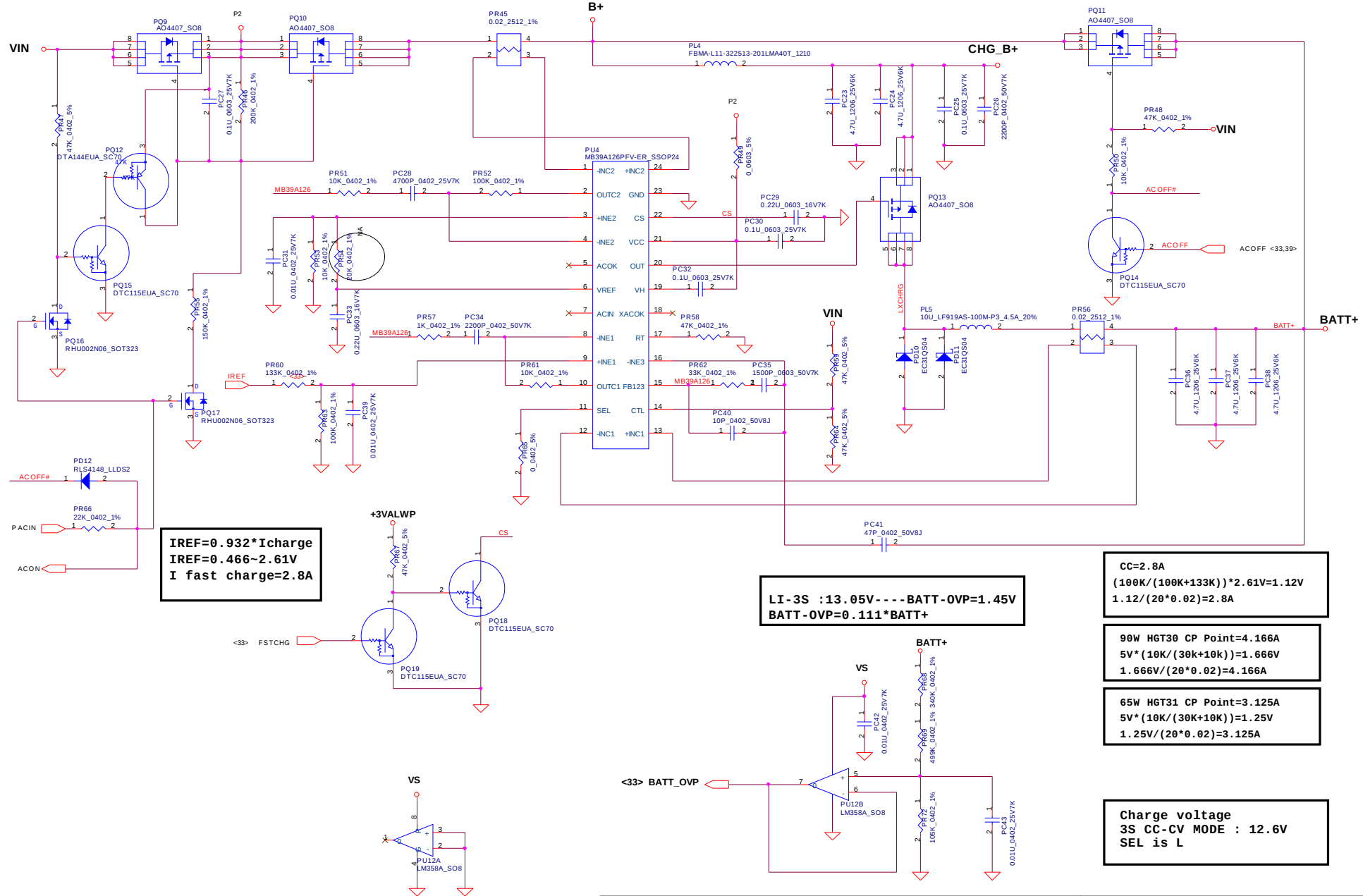


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65W PR45=0.02_2512_1% PR54=30K_0402_1% Iadp=0~3.125A
90W PR45=0.02_2512_1% PR54=20K_0402_1% Iadp=0~4.166A

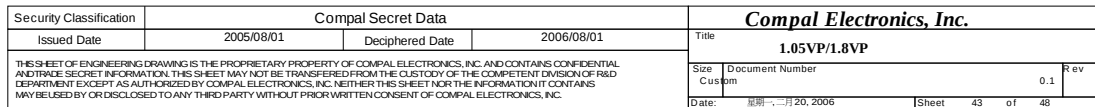
Fosc=14100/Rt=14100/47=300KHz

Charger

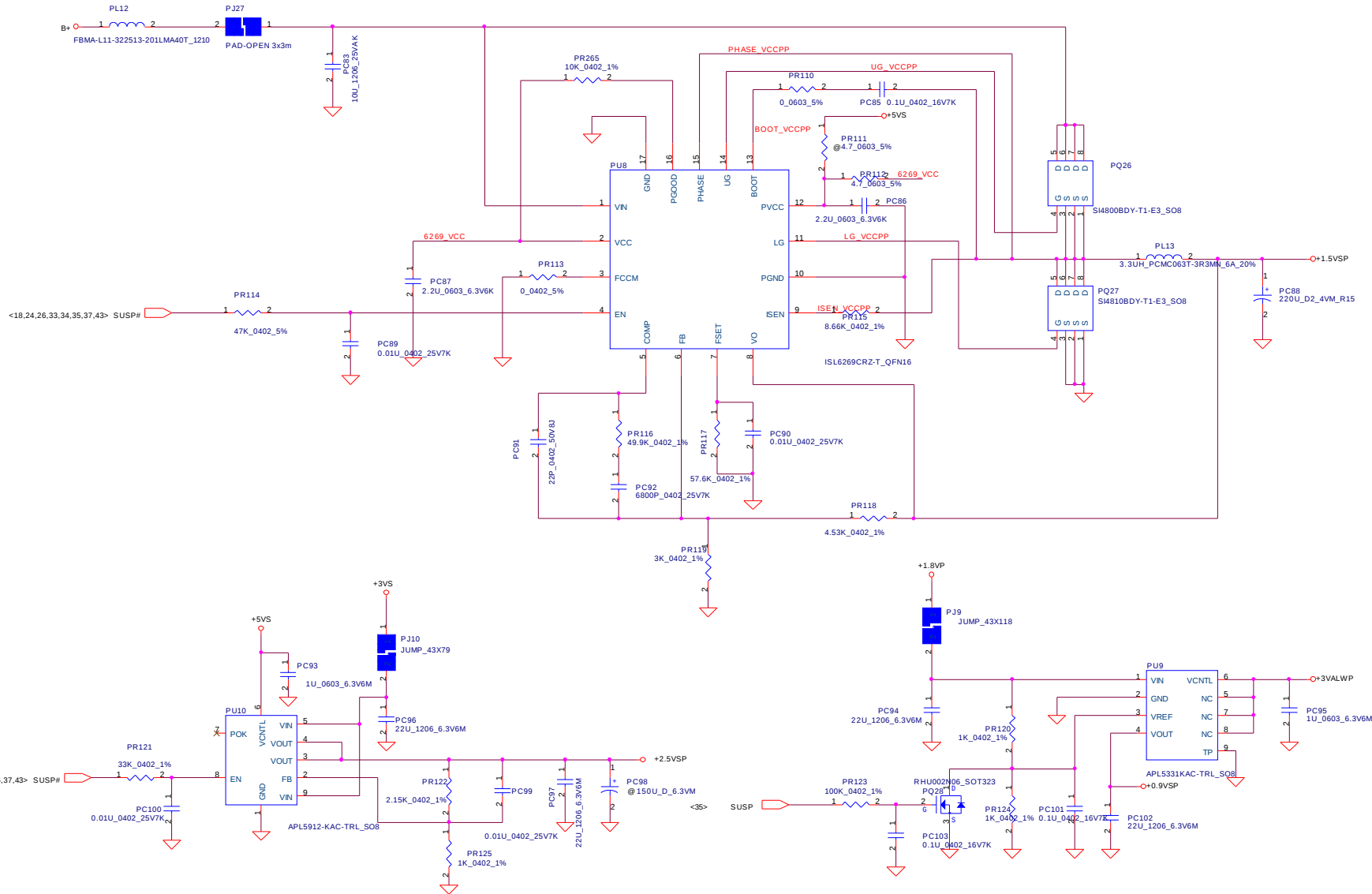


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+1.05VSP Ilimit=6.33A~10.03A



+1.5VSP Ilimit = 9.38A-12.5A



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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	VER	Phase
1		MODIFY 3V/5V current limit to 6.5A~8.1A/6.5A to 10.2A		42	MODIFY PR83/PR84 FROM 499K TO 374K		DVT
2		ADD or decrease CPU CORE ring with EMI solution : snubber		45	Reserve PR224//PR256: 4.7 1206 ,add PC167/PC182:680P		DVT
3		Reserve PR267,PR268 seperate in CPU CORE high side gate for EMI require		45	Reserve PR267,PR268:0 0603		DVT
4		change PJP1 from 5 pin to 4 pin		39	change PJP1 from 5 pin to 4 pin		DVT
5		modify sequecce		43	change PR179 to 100k, PC132 =0.1U		DVT
6		modify Vgate		45	add PQ38:RHU002N06,PR240:2K,delete PR247		
7							
8							
9							
10							
11							
8							
9							

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Version change list (P.I.R. List)

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Item	Fixed Issue	Rev.	PG #	Modify List	B.Ver #	Phase
1	Add EC_Port80 Signals to DDR2 DIMM1 & DIMM2	0.2	P.13 P.14	1.Connect U6.91 (EC_P80_CLK) through a 0 Ohm R to JP3.83 & JP4.83 2.Connect U6.92 (EC_P80_DATA) through a 0 Ohm R to JP3.69 & JP4.69	0.2	DVT
2	Impedance not match for both CRT & TV Out	0.2	P.17	R3, R4, R5, R6, R7, R8 Change from NC to 150 Ohm	0.2	DVT
3	LCD Panel will flash white frame when power on	0.2	P.16	no stuff D10 (CH751H), stuff R204 (100K)	0.2	DVT
4	ICH7's GPIO configuration modification	0.2	P.21	GPIO10 connect to ACIN GPIO7 connect to G7X_THER_ALERT# GPIO39 connect to KILL_MDC#	0.2	DVT
5	<New Add> MDC supports S4/S5 resuming	0.2	P.28	MDC power connection change to +3VALW from +3VS	0.2	DVT
6	Audio Circuit modification for : 1. Line-Out connection change from Pin.35/Pin.36 to Pin.43/Pin.45 2. Audio-OUT Auto-Switch by HP Plugging In 3. MicPhone Noise Reduction 4. Cleared off B0 Sound from both entry of Windows XP & Power Off	0.2	P.29-31	Line-Out connection change from Pin.35/Pin.36 to Pin.43/Pin.45 Connect Pin.32 (LFE_OUT) through 2 1uF Cap to Pin.43/Pin.45 +Audio_VREF_LF connection change to 1/2 +AVDD_AC97 Int.MIC connection changes to Pin31/Pin32 through 1uF for each New Add a JACK_PLUG_MIC signal from MIC JACK EAPD signal connect to EC's GPIO4B APA2068's I3PIN(SE/BTL#) connect to GND	0.2	DVT
7	EC GPIO configuration modification	0.2	P.33	New add Port80 information OUT from Pin34(CLK), pin35(DATA) LED4 connection changes from GPIO17(35 PIN) to GPIO4A(91 PIN) New Add DAC's EAPD connect to EC's GPIO4B (92PIN). SKU_ID (GPIO3B) Changes to BRD_ID New Add WL_OFF# (GPIO1F, 46PIN) New Add BT_OFF# (GPIO50, 84PIN) New Add TP_ACT_LED# (GPIO3F, 80PIN) New Add TP_LOCK_LED# (GPIO12, 30PN)	0.2	DVT
8	Lid Switch changes from USB BD to M/B	0.2	P.37	Circuit of Lid SW changes from USB BD to M/B (DEL Lid SW on USB BD)	0.2	DVT
9	Blue LED too dark when active due to VF too High on blue LED	0.2	P.37-38	Changes LED power from +3VS(+3VALW) to +5VS(+5VALWS)	0.2	DVT
10	New Add LED Buffer for LED4, TP_LOCK_LED#, TP_ACT_LED#	0.2	P.37 P.38	TP_ACT_LED# connect to Q802.2, and Q802.1 to GND, then connect to LED804 through a 220 Ohm R TP_LOCK_LED# connect to Q803.2, and Q802.1 to GND, then connect to LED805 through a 220 Ohm R EC_GPIO4A connect to Q804.2, and Q804.1 to GND, then connect to R283 (220 Ohm)	0.2	DVT
11	leakage of electricit when System is running S3 mode	0.2		NC For R458, R402, R411, R128, R831, R829	0.2	DVT

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Item	Fixed Issue	Rev.	PG #	Modify List	B.Ver #	Phase
12	GIGA LAN function failed for both Loopback or PXE on RTL8110SCL solution	0.3	P.27	1. Add a R734 (0 Ohm) resistor between +2.5V_LAN & VTCT for MAC 2. Removed all of the bypass Cap.(C398, C396, C418, C408) for MAC's TCT pins 3. Removed all of pulled down resistors (49.9 Ohm) & Cap.(0.01u)	0.3	PVT
13	Subwoofer still make POP Sound	0.3	P.31	1. Add 0 Ohm resistors, R732 (0 Ohm) connection between AMP_OFF# & U12.2 (SD#) for reserved 2. a 0 Ohm connection between EAPD & U12.2(SD#)	0.3	PVT
14	Mic Switch between Int. & Ext. be Failed	0.3	P.29	1. R717.1 Disconnect from U11.17 2. R717.1 connect to U11.16	0.3	PVT
15	Wrong parts	0.3	P.35	Change package of C434, C224 & C312 from 0402 to 0603	0.3	PVT
16	Add a discharging path of +3.3VS	0.3	P.35	1. Connect +3.3VS to R731.1 2. Connect R731.2 to Q704.1 3. Connect Q704.2 to NET : SUSP signal 4. Connect Q704.3 to GND	0.3	PVT

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